SECTION 16731
MODEL 2070 CONTROLLER UNIT

PART 1 GENERAL

1.01 SECTION INCLUDES

A. This specification defines the minimum detailed requirements applicable to the Type 2070 Advanced Transportation Controller (ATC) unit. The Advanced Transportation Controller (ATC) is a general purpose programmable controller that is intended for continuous unattended operation in harsh environments.

B. This specification defines specific, interchangeable modules that are combined to form a Type 2070 ATC that is capable of running control software that might be provided from a variety of providers. This specification defines several module options that can be arranged in a variety of composition configurations to meet the needs of the user.

C. This specification lays out compositions for Full, NEMA, Lite, and ITS configurations. The Type 2070 version of the ATC is designed such that all components are fully standardized and are therefore interchangeable.

1.02 UNIT PRICES

A. Measurement

This Item will be measured as each traffic signal controller unit furnished.

B. Payment

The materials furnished in accordance with this Item and measured as provided under “Measurement” as each specified controller unit furnished.

1.03 WARRANTY

A. All materials furnished will be warranted by the supplier for a period of two (2) years from date of delivery.

1.04 CONTROLLER DESCRIPTIONS

A. Controller Housing. The Type 2070 controller defines a controller housing that is intended to fit an EIA 19 in. rack mounted form commonly found in the Type 332 and ITS family of cabinets. A NEMA base module is defined for those NEMA TS1 and TS2 shelf mounted applications.

B. CPU Module. The CPU module consists of the main CPU, memory, software and interfaces to the remainder of the controller. There are three CPU module configurations identified in this standard. The Type 2070-1A is a two-board configuration that has a VME-based CPU board and a Transition Board. The Type 2070-1B configuration consists of a single board module. The Type 2070-1C configuration is intended to interface with the “engine board” specified by the ATC v5.2 standard.

C. Field I/O Module. The Field I/O Module provides a mechanism for input and output interfaces. There are three options for the Field I/O Module. The Type 2070-2A Modules is intended to provide a parallel I/O interface with the Type 332 family of cabinets using the C1S connector. The Type 2070-2B Module is intended to provide a serial I/O interface to the ITS cabinet family and the NEMA interface to TS1 cabinets. The Type 2070-2N is for the NEMA TS2 Type 1 cabinets.

D. Front Panel Module. A controller Front Panel usually contains a keyboard and display that comprise the user field interface. The Front Panel on the Type 2070 controller is optional. This standard identifies three front panel options: the Type 2070-3A Front Panel includes a large character (4 lines of 40 characters) Liquid Crystal Display (LCD), the Type 2070-3B Front Panel includes a small character (8 lines of 40 characters) LCD, and the Type 2070-3C contains only a serial connection for interfacing with a notebook computer or some other handheld computing device.

E. Power Supply Module. A power supply module is used to convert 120 volt power to voltages required to operate the electronics inside the Type 2070 controller unit. This power supply must meet certain minimum electrical characteristics defined herein for its intended use. This standard identifies four options for the Power Supply: The Type 2070-4A identifies a 10 ampere power supply that is needed for those cases there is a need to support the VME cage assembly, and the Type 2070-4B identifies a 3.5 ampere power supply that is typically used in the “Lite” controller configurations. The Type 2070-4N (A and B) identifies the corresponding power supplies needed to support the NEMA TS1 and TS2 standards. This, however, does not preclude a Manufacturer or a DEPARTMENT from requiring a specific power supply form factor so that it is consistent across a wide range of packages that may be employed by that DEPARTMENT.

F. VME Cage Assembly. The VME Cage Assembly is an optional expansion module for the Type 2070 ATC. The Type 2070-5 consists of a five-slot 3U VME card rack. The use of the VME Cage Assembly requires the use of the Type 2070-4A 10-ampere power supply.

G. Communications Modules. This standard includes a variety of serial and modem communications modules. The 2070-6 series of modules are for internal modems and the Type 2070-7 series of modules are for serial communications.

H. NEMA Interface. This standard includes requirements for an optional module to interface with the NEMA TS1 and NEMA TS2 Type 2 cabinets. The Type 2070-8 NEMA Field I/O Module is an external module that attaches to the bottom of the 2070 and provides for the typical “A,” “B,” and “C” NEMA connectors.

1.05 CONTROLLER REQUIREMENTS

A. General. All furnished equipment must be new and unused. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) must not be used.

B. Controller Configurations. Controller Versions provided here are EXAMPLES of possible Controller Configurations.

		2070L	2070 LS	2070 LC	2070 LCS	2070 N1	2070 N2	2070 N2C
	ASSOCIATED DEVICES							
1	Type 2070-1A CPU Module					1		
2	Type 2070-1B CPU Module	1	1				1	
3	Type 2070-1C CPU Module			1	1			1
4	Type 2070-2A Field I/O Module	1		1				
5	Type 2070-2B Field I/O Module		1		1	1	1	1
6	Type 2070-3 Front Panel Assy.	1	1	1	1	1	1	1
7	Type 2070-4A Power Supply	1	1	1	1			
8	Type 2070-4AN Power Supply					1	1	1
9	Type 2070-5 VME Cage Assy.							
10	Type 2070-8 NEMA Base					1	1	1
11	Type 2070-2N Field I/O Module						1	1
12	Type 2070-6 Comm Module							
13	Type 2070-7 Comm Module	1*	1*					

* Indicates Optional Units for any configuration.

2070 L is a basic configuration currently using the 1B CPU Module.

2070 LS is the basic L version that replaces the 2A FIO with a 2B communication interface to drive the serial cabinet.

2070 LC and LCS are the same units using the 1C CPU Module.

2070N versions include 1A, VME ,1B and 1C CPU Modules. The 2N Field I/O module is designed to replace the 2070-8 NEMA Base and use the TS2 serial interface.

1.06 DOCUMENTATION

A. Manuals. Two copies of Manual Documentation must be supplied for each item purchased. The manual must be bound in durable covers made of either 65-pound stock paper or clear plastic. The manual must be printed on 8-1/2 in. by 11 in. paper, with the exception that schematics, layouts, parts lists and plan details may be on 11 in. by 17 in. sheets, with each sheet neatly folded to 8-1/2 in. by 11 in. size. A minimum of Times New Roman or Arial 10 point font must be used for all manual text, excluding drawings and schematics. Drawing text may use a smaller font size.

1. Manual Contents. Each manual must include the following sections in the order listed:

   a. Table of Contents

   b. Glossary

   c. Manufacturer Contact Information
      Address
      Telephone Number
      Fax Number
      General Email Address

   d. General Description

   e. General Characteristics

   f. Installation

   g. Adjustments

   h. Theory of Operation
      Systems Description (include block diagram).
      Detailed Description of Circuit Operation.

   i. Maintenance
      Preventive Maintenance.
      Trouble Analysis.
      Trouble Shooting Sequence Chart.
      Wave Forms.
      Voltage Measurements.
      Alignment Procedures.

   j. Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer,

data specification sheets for special design components and original manufacturer's part number).

k. Electrical Interconnection Details & Drawings.

l. Schematic and Logic Diagram

m. Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part.

n. The date, serial numbers, model numbers and revision numbers of equipment covered by the manuals must be printed on the front cover of the manuals.

2. Draft Manual. A preliminary draft of the manual must be submitted, when required, to the CITY OF HOUSTON for approval prior to final printing.

B. Packaging. Each item delivered must be individually packed in its own shipping container. When loose Styrofoam is used for packing the item, the item must be sealed in a plastic bag to prevent direct contact with the Styrofoam.

C. Delivery. Each item delivered for testing must be complete, including manuals, and ready for testing.

D. Metals. All sharp edges and corners must be rounded and free of any burrs.

1. Aluminum. Sheet must be 63 gauge American Standard (0.060-in.) minimum thick Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded must be Type 6061-T6, or equal.

2. Stainless Steel. Sheet must be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

3. Cold Rolled Steel. Sheet, Rod, Bar and Extruded must be Type 1018/1020.

a. Plating. All cold roll steel must be plated. All plating must be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class I or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.

E. Mechanical Hardware. All bolts, nuts, washers, screws, hinges and hinge pins must be stainless steel unless otherwise specified.

F. Electrical Isolation. Within the circuit of any device, module, or Printed Circuit Board (PCB), electrical isolation must be provided between DC logic ground, equipment ground and the AC- conductor. They must be electrically isolated from each other by 500 megohms, minimum, when tested at the input terminals with 500 VDC.

G. Daughter Boards. Keyboards and LCD/LED Displays are considered daughter boards. Daughter boards must be mechanically secured with a minimum of

four spacers/metal screws. Connectors must be either Flat Cable or PCB Headers. Components are to be mounted under the daughter board.

PART 2 PRODUCTS

2.01 COMPONENTS

A. General. All components must be second sourced and must be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer. When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component must be furnished with each 20, or fraction thereof, components used. The electronic circuit design must be such that all components of the same generic type, regardless of manufacturer, must function equally in accordance with the specifications.

B. Electronic Components.

1. No device to be socket mounted unless specifically called out.

2. No component to be operated above 80% of its maximum rated voltage, current or power ratings. Digital components must not be operated above 3% over their nominal voltage, current or power ratings.

3. No component to be provided where the manufactured date is three years older than the contract award date. The design life of all components, operating for twenty-four hours a day and operating in their circuit application, must be ten years or longer.

4. Components must be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, a clamp, fastener, retainer, or hold-down bracket must support the component mechanically.

5. The Manufacturer must submit detailed engineering technical data on all components at the request of the City of Houston. The Manufacturer must certify that the component application meets the requirements of this standard.

C. Capacitors. The DC and AC voltage ratings as well as the dissipation factor of a capacitor must exceed the worst-case design parameters of the circuitry by 150%. Capacitor encasements must be resistant to cracking, peeling and discoloration. All capacitors must be insulated and must be marked with their capacitance values and working voltages. Electrolytic capacitors must not be used for capacitance values of less than 1.0 microfarad and must be marked with polarity.

D. Potentiometers. Potentiometers with ratings from 1 to 2 watts must meet Military Type RV4 requirements. Under 1 Watt potentiometers must be used

only for trimmer type function. The potentiometer power rating must be at least 100% greater than the maximum power requirements of the circuit.

E. Resistors. Fixed carbon film, deposited carbon, or composition-insulated resistors must conform to the performance requirements of Military Specifications MIL-R-11F or MIL-R-22684. All resistors must be insulated and be marked with their resistance values. Resistance values must be indicated by the EIA color codes, or stamped value. The value of the resistors must not vary by more than 5% between -37 degrees C and 74 degrees C.

1. Special ventilation or heat sinking must be provided for all 2- watt or greater resistors. They must be insulated from the PCB.

F. Semiconductor Devices.

1. All transistors, integrated circuits, and diodes must be a standard type listed by EIA and clearly identifiable.

2. All metal oxide semiconductor components must contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

3. Device pin "1" locations must be properly marked on the PCB adjacent to the pin.

G. Transformers and Inductors. All power transformers and inductors must have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination. All transformers and inductors must have their windings insulated, be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

H. Triacs. Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC must be mounted to a heat sink with thermal conductive compound or material, in addition to being mechanically secured.

I. Circuit Breakers. Circuit breakers must be listed by UL or ETL. The trip and frame sizes must be plainly marked (marked on the breaker by the manufacturer), and the ampere rating visible from the front of the breaker. Contacts must be silver alloy and enclosed in an arc-quenching chamber. An ambient air temperature range of from -18 degrees C to 50 degrees C must not influence overload tripping. The minimum Interrupting Capacity must be 5,000 amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity. For circuit breakers 80 amperes and above, the minimum interrupting capacity must be 10,000 amperes, RMS. Circuit breakers must be the trip-free type with medium trip delay characteristic (Carlingswitch Time Delay Curve #24 or equal).

1. Load Circuit Breaker Auxiliary Internal Switches. The Load Circuit Breakers used to power Switch Packs must have auxiliary switches. The auxiliary

switches must “open” when the load breaker has tripped and the system will transfer the power from the Main Contactor to the Flash or Blank condition.

J. Fuses. All Fuses that are resident in a bayonet style fuse holder must have the fuse size rating labeled on the holder or on the panel adjacent to the holder. Fuses must be easily accessible and removable without use of tools.

K. Switches.

1. Dip. Dual-inline-package, quick snap switches must be rated for a minimum of 30,000 operations per position at 50 milliamperes, 30 VDC. The switch contact resistance must be 100 milliohms maximum at 2 milliamperes, 30 VDC. The contacts must be gold over brass.

2. Logic. The switch contacts must be rated for a minimum of 1-ampere resistive load at 120 VAC and must be silver over brass (or equal). The switch must be rated for a minimum of 40,000 operations.

3. Control. The switch contacts must be rated for a minimum of 5 amperes resistive load at 120 VAC or 28 VDC and be silver over brass (or equal). The switch must be rated for a minimum of 40,000 operations.

4. Power. Ratings must be the same as CONTROL, except the contact rating must be a minimum of 10 amperes at 125 VAC.

L. Terminal Blocks. The terminal blocks must be barrier type, rated at 20 amperes and 600 VAC RMS minimum. The terminal screws must be 0.3125 in. minimum length nickel-plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

M. Screw Lug and Cam Driven Connectors. Provided the connectors mate, screw lug cam driven devices or crimp pin connectors must be allowable if the interface is part of a harness. For field termination, screw lug and cam driven assemblies are interchangeable for field wiring termination, provided they both accommodate 22-gauge wire on the inputs and 22-gauge wire on the outputs.

N. Wiring, Cabling and Harnesses.

1. Harnesses must be neat, firm and properly bundled with external protection. They must be tie-wrapped and routed to minimize crosstalk and electrical interference. Each harness must be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements. Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring.

2. Wiring containing AC must be bundled separately or shielded separately from all DC logic voltage control circuits.

3. Wiring must be routed to prevent conductors from being in contact with metal edges. Wiring must be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

4. All conductors, except those that can be readily traced, must be labeled. Labels attached to each end of the conductor must identify the destination of the other end of the conductor.

5. All conductors must conform to MIL-W-16878E/1 or better and have a minimum of 19 strands of copper. The insulation must be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor must conform to MIL-W-16878/17.

6. Conductor color identification must be as follows:

   AC- circuits – white

   Equip. Ground - solid green or continuous green color with 1 or more yellow stripes

   DC logic ground - continuous white with a red stripe

   AC+ circuits - continuous black or black with colored stripe

   DC logic ungrounded or signal - any color not specified

O. Indicators and Character Displays.

1. All indicators and character displays must be readily visible at a radius of up to 4 feet within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 degrees (+/-2 degrees) to the front panel.

2. All indicators and character displays must have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators must be self-luminous. All indicators must have a rated life of 100,000 hours minimum. Each LED indicator must be white or clear when off. Indicators supplied on equipment requiring handles must be mounted such that a horizontal clearance is provided.

3. Liquid Crystal Displays (LCD) must be readable at temperatures of -20 degrees C to +70 degrees C. All controller unit functions are required to operate at temperatures of –37 degrees C to +74 degrees C.

P. Connectors. Connectors must be keyed to prevent improper insertion of the wrong connector where equipment damage or operator injury may result. The mating connectors must be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).

1. Type T. Type T connector must be a single row, 10 position, feed through terminal block. The terminal block must be a barrier type with 6-32, 0.25 in. or longer, nickel plated brass binder head screws. Each terminal must be permanently identified as to its function.

2. Plastic Circular and Type M. Pin and socket contacts for connectors must be beryllium copper construction subplated with 1.27 microns nickel and plated with 0.76 microns gold. Pin diameter must be 0.0618 in. All pin and socket connectors must use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool or equal.

3. Card Edge and Two Piece PCB.

   a. Edge connectors must have bifurcated gold-plated contacts. The PCB receptacle connector must meet or exceed the following:

      Operating Voltage: 600 VAC (RMS)

      Current Rating: 5.0 Amperes

      Insulation Material: Diallyl Phthalate or Thermoplastic

      Insulation Resistance: 5,000 Megohms

      Contact Material: Copper alloy plated with 0.00005 in. of nickel and 0.000015 in. of gold

      Contact Resistance: 0.006 Ohm maximum

   b. The two-piece PCB connector must meet or exceed the DIN 41612.

   c. The PCB 22/44 Connector must have 22 independent contacts per side; dual sided with 0.156 in. contact centers.

4. Wire Terminal. Each wire terminal must be solderless with PVC insulation and a heavy-duty short -locking spade type connector. Crimp terminal connectors using a Controlled-Cycle type crimping tool.

5. Flat Cable. Each flat cable connector must be designed for use with 26 AWG cable; have dual cantilevered phosphor bronze contacts plated with 0.00015 in. of gold over 0.00005 in. of nickel; and have a current rating of 1 Ampere minimum and an insulation resistance of 5 Megohms minimum.

6. PCB Header Post. Each PCB header post must be 0.025 in. square by 0.3425 in. high from the plane of the PCB to the end of the pin; be mounted on 0.10 in. centers; and be tempered hard brass plated with 0.00015 in. of gold over 0.00005 in. of nickel.

7. PCB Header Socket. Each PCB header socket block must be nylon or diallyl phthalate. Each PCB header socket contact must be removable, but crimp-connected to its conductor. List the part number of the extraction tool

recommended by its manufacturer. Each PCB header socket contact must be brass or phosphor bronze plated with 0.0015 in. of gold over 0.00005 in. of nickel.

Q. Surge Protection Device. The surge suppression device must comply with ANSI/IEEE C62.41 (100 Kilohertz Ring Wave, the 1.2/50 microseconds – 8/20 Combination Wave and the EFT Burst) at voltages and currents specified at “Location Category B2” and at “Test Severity” level III (i.e. up to 4.0 Kilovolts, open-circuit).

2.02 MECHANICAL REQUIREMENTS

A. Assemblies. All assemblies must be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs. Assemblies must be provided with two guides for each plug-in PCB or associated device (except relays). The guides must extend to within 0.75 in. from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, attach the guides securely to the file or assembly chassis.

B. Locking Devices. All screw type fasteners must utilize locking devices or locking compounds except finger screws, which are captive.

C. PCB Design and Connectors. No components, traces, brackets or obstructions are to be within 0.125 in. of the board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number must appear and be readily visible on all PCBs.

D. Model and Serial Numbers.

1. The manufacturer's model number, and circuit issue or revision number must appear on the rear panel of all equipment supplied (where such panel exists). In addition to any assignment of model numbers by the manufacturer, the TYPE number must be displayed on the front panel in bold type, at least 0.25 in. high.

2. A permanent label must be affixed to the inside near and center floor of the Type 2070 unit chassis when viewed from the front. The label must display the unit's serial number and be permanent and easy to read.

E. Workmanship. Workmanship must conform to the requirements of this specification and be in accordance with the highest industry standards.

F. Tolerances. The following tolerances must apply, except as specifically shown on the plans or in these specifications:

TYPE	DIMENSIONAL TOLERANCE
Sheet Metal	+/-0.0525 in.
PCB	+0 in., - 0.010 in.
Edge Guides	+/-0.015 in.

*Note: These dimensional tolerances do not apply to material gauge or thickness.

2.03 ENGINEERING

A. Human Engineering. The equipment must be engineered for simplicity, ease of operation and maintenance.

1. Knobs must be a minimum of 0.5 in. in diameter and a minimum separation of 0.5 in. edge to edge.

2. PCBs must slide smoothly in their guides while being inserted into or removed from the frame and fit snugly into the plug-in PCB connectors. PCBs must require a force no less than 5 pounds-force or greater than 50 pounds-force for insertion or removal.

B. Design Engineering. The design must be inherently temperature compensated to prevent abnormal operation. The circuit design must include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range. The design must take into consideration the protection of personnel from all dangerous voltages.

C. Generated Noise. No item, component or subassembly is to emit an audible noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly is to emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.

2.04 PRINTED CIRCUIT BOARDS

A. Design, Fabrication and Mounting.

1. All contacts on PCBs must be plated with a minimum thickness of 0.00003 in. gold over a minimum thickness of 0.000075 in. nickel.

2. PCB design must be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.

3. Fabrication of PCBs must be in compliance with Military Specification MIL-P-13949, except as follows:

a. NEMA FR-4 glass cloth base epoxy resin copper clad laminates 0.0625 in. minimum thickness must be used. Inter-component wiring must be by laminated copper clad track having a minimum weight of 0.2 ounces per square foot with adequate cross section for current to be carried. All copper tracks must be plated or soldered to provide complete coverage of all exposed copper tracks. Jumper wires to external PCB components must be from plated-through padded holes and as short as possible.

b. All PCBs must conform to Section 3.3 of Military Specification MIL-P-13949G Grade of Pits and Dents and be of Grade B quality (3.5.1.3) or better. The class of permissible bow or twist must be Class C (Table V) or better. The class of permissible warp or twist must be Class A (Table II) or better.

c. Omit Sections 4.2 through 6.6 of Military Specification MIL-P-13949G (inclusive) except as referenced in previous sections of this specification.

d. The mounting of parts and assemblies on the PCB must conform to Military Specification MIL-STD-275E, except as follows:

(1) Semiconductor devices that dissipate more than 250 milliwatts or cause a temperature rise of 10 degrees C or more must be mounted with spacers, transipads or heat sinks to prevent contact with the PCB.

(2) When completed, remove all residual flux from the PCB.

(3) The resistance between any two isolated, independent conductor paths must be at least 100 Megohms when a 500 VDC potential is applied.

(4) All PCBs must be coated with a moisture resistant coating.

(5) Where less than 0.25 in. lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.0625 in. (+/-0.0005 in.) Thick Mylar (polyester) plastic cover must be provided on the metal to protect the PCB.

e. Each PCB connector edge must be chamfered at 30 degrees from board side planes. The key slots must also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots must be 0.045 in. (+/-0.005 in.) for 0.1 in. spacing and 0.055 in. (+/-0.005 in.) for 0.156 in. spacing.

B. Soldering.

1. Hand soldering must comply with Military Specification MIL-STD-2000.

2. Automatic flow soldering must be a constant speed conveyor system with the conveyor speed set at optimum to minimize solder peaks or points. Temperature must be controlled to within +/- 8 degrees C of the optimum temperature. The soldering process must result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process. Wherever clinching is not used, provide a method of holding the components in the proper position for the flow process.

3. If exposure to the temperature bath is of such a time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component must be hand soldered to the PCB after the flow process has been completed.

C. Definitions. Definitions for the purpose of this section on PCBs must be taken from MIL-P-55110D Section 3.3 and any current addendum.

D. Jumpers. Jumpers are not allowed unless called out in the specifications or approved by the City of Houston.

2.05 QUALITY CONTROL

A. Components. All components must be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

B. Subassembly, Unit or Module. Complete electrical, environmental and timing compliance testing must be performed on each module, unit, printed circuit or subassembly. Components will be tested as a complete controller assembly. Housing, chassis, and connection terminals must be inspected for mechanical sturdiness, and harnessing to sockets to be electrically tested for proper wiring sequence. The equipment must be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

C. Pre-delivery Repair.

1. Any defects or deficiencies found by the inspection system involving mechanical structure or wiring must be returned through the manufacturing process or special repair process for correction.

2. PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Do not flow solder a PCB more than twice.

3. Hand soldering is allowed for printed circuit repair.

2.06 ELECTRICAL, ENVIRONMENTAL AND TESTING REQUIREMENTS

The framework of this section, along with the specific test requirements contained herein, is excerpted with modifications from NEMA TS2-2003 - Section 2 by permission of NEMA. Excerpt © 2002 AASHTO / ITE / NEMA.

A. General. This section establishes the limits of the environmental and operational conditions in which the Controller Assembly will perform. This section defines the minimum test procedures that may be used to demonstrate conformance of a device type with the provisions of the standard. These test procedures do not verify equipment performance under every possible combination of environmental requirements covered by this standard. Nothing in this testing profile must be construed as to relieve the requirement that the

equipment provided must fully comply with these standards/specifications under all environmental conditions stated herein.

The City of Houston may wish to extend the testing profile or introduce additional tests to verify compliance. (Authorized Engineering Information).

B. Inspection. A visual and physical inspection must include mechanical, dimensional and assembly conformance to all parts of this standard.

C. Testing Certification.

1. A complete quality control / final test report must be supplied with each item. Quality control procedures must be submitted to the City of Houston prior to production. The test report must indicate the name of the tester and be signed by a responsible manager.

2. The quality control procedure and test report format must be supplied to the City of Houston for approval upon request. The quality control procedure must include the following, in the order shown:

   (a) Design Acceptance testing of all supplied components.

   (b) Physical and functional testing of all modules and items.

   (c) Environmental testing reports for all equipment.

   (d) Physical and functional testing of all items.

3. Separate certifications must be provided for Design and Production. Design Acceptance testing must be performed with a fully loaded and functional Cabinet Assembly. Production testing must be performed as part of the City of Houston's procurement delivery procedures and that testing should be performed at the Major Unit level. (Authorized Engineering Information).

4. Certain portions of the test procedures contained in this standard my cause damage to the unit (e.g. protection devices may be aged) and are not recommended for routine Production testing. (Authorized Engineering Information)

D. Definitions of Major Units of the Cabinet Assembly. For the purpose of this section, "Major units of the Cabinet Assembly" must include the Controller Unit, Application Software for implementing the desired functionality, Cabinet Monitor Unit (CMU), Auxiliary Monitor Unit (AMU), Serial Interface Units (SIUs), Power Distribution Unit (PDA), Switch Packs, Flasher(s), and Detector(s).

E. Environmental and Operating Requirements. The requirements (voltage, temperature, etc.) of this section must apply in any combination.

1. Voltage and Frequency.

a. Operating Voltage. The nominal voltage must be 120 VAC, unless otherwise noted.

b. Operating Frequency. The operating frequency range must be 60 hertz (+/-3.0 hertz), unless otherwise noted.

2. Transients, Power Service. The Test Unit must maintain all defined functions when the independent test pulse levels specified below occur on the alternating-current power service.

a. High Repetition Noise Transients.

(1) The test pulses must not exceed the following conditions:

(a) Amplitude: 300 Volts, both positive and negative polarity.

(b) Peak Power: 2500 watts.

(c) Repetition: 1 pulse approximately every other cycle moving uniformly over the full wave in order to sweep across 360 degrees of the line cycle once every 3 seconds.

(d) Pulse Rise Time: 1 microsecond.

(e) Pulse Width: 10 microseconds.

(f) This test is performed without protection in place or operational.

This test is considered to be a minimum test requirement for the Test Unit complying with ANSI/IEEE C62.41. Regional conditions may warrant additional testing as described in ANSI/IEEE C62.41. (Authorized Engineering Information)

b. Low Repetition High Energy Transients.

(1) The test pulses must not exceed the following conditions:

(a) Amplitude: 600 Volts (+/-5 percent), both positive and negative polarity.

(b) Energy Source: Capacitor, oil filled, 10 microfarads (+/-10 percent), internal surge impedance less than 1 ohm.

(c) Repetition: 1 discharge every 10 seconds.

(d) Pulse Position: Random across 360 degrees of the line cycle.

(e) This test is performed with protection in place and operational.

This test is considered to be a minimum test requirement for the Test Unit complying with ANSI/IEEE C62.41. Regional conditions may warrant additional testing as described in ANSI/IEEE C62.41. (Authorized Engineering Information)

c. Nondestructive Transient Immunity.

(1) The Test Unit (with protection in place and operational) must be capable of withstanding a high energy transient having the following characteristics repeatedly applied to the alternating current input terminals (no other power connected to terminals) without failure of the test specimen:

(a) Amplitude: 1000 Volts (+/-5 percent), both positive and negative polarity.

(b) Energy Source: Capacitor, oil filled, 15 microfarads (+/-10 percent), internal surge impedance less than 1 ohm.

(c) Repetition: Applied to the Test Unit once every 2 seconds for a maximum of three applications for each polarity.

(d) After the foregoing, the Test Unit must perform all defined functions upon the application of nominal alternating current power.

This test is considered to be a minimum test requirement for the Test Unit complying with ANSI/IEEE C62.41 (100 Kilohertz Ring Wave, the 1.2/50 microseconds – 8/20 Combination Wave and the EFT Burst) at voltages and currents specified at "Location Category B2" and at "Test Severity" level III (i.e. up to 4.0 Kilovolts, open-circuit). Regional conditions may warrant additional testing as described in ANSI/IEEE C62.41. (Authorized Engineering Information)

d. Transients, Input-Output Terminals.

(1) The Test Unit (without protection in place or operational) must maintain all defined functions, when the test pulse occurs on the input-output terminals.

(a) Amplitude: 300 Volts, both positive and negative polarity.

(b) Pulse Source: 1000 ohms nominal impedance.

(c) Repetition: 1 pulse per second, for a minimum of 5 pulses per selected terminal.

(d) Pulse rise time: 1 microsecond.

(e) Pulse width: 10 microseconds.

This test is considered to be a minimum test requirement for the Test Unit complying with ANSI/IEEE C62.41. Regional conditions may warrant additional testing as described in ANSI/IEEE C62.41. (Authorized Engineering Information)

e. Temperature and Humidity. The Test Unit must maintain all programmed functions when the temperature and humidity ambients are within the specified limits defined herein.

(1) Ambient Temperature.

(a) The operating ambient temperature range must be from -37 degrees C to +74 degrees C. The storage temperature range must be from -45 degrees C to +85 degrees C.

(b) The rate of change in ambient temperature must not exceed 18 degrees C per hour, during which the relative humidity must not exceed 95 percent.

(2) Humidity.

(a) The relative humidity must not exceed 95 percent non-condensing over the temperature range of -37 degrees C to +74 degrees C.

(b) Above +46 degrees C, constant absolute humidity must be maintained. This will result in the relative humidity shown in Exhibit 3-1 for dynamic testing.

Table 1
AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY
AT BAROMETRIC PRESSURES (29.92 In. Hg.) (NON-CONDENSING)

Ambient Temperature/ Dry Bulb (in degrees C)	Relative Humidity (in percent)	Ambient Temperature/ Wet Bulb (in degrees C)
-37.0 to 1.1	10	-17.2 to 42.7
1.1 to 46.0	95	42.7
48.8	70	42.7
54.4	50	42.7
60.0	38	42.7
65.4	28	42.7
71.2	21	42.7
74.0	18	42.7

F. Test Facilities. All instrumentation required in the test procedures, such as voltmeters, ammeters, thermocouples, pulse timers, etc. must be selected in accordance with good engineering practice. In all cases where time limit tests are required, the allowance for any instrumentation errors must be included in the limit test.

1. Variable Voltage Source: A variable source capable of supplying 20 amperes from 100 VAC to 135 VAC.

2. Environmental Chamber: An environmental chamber capable of attaining temperatures of -37 degrees C to +74 degrees C and relative humidity given in Table 1.

3. Transient Generators: Transient generators capable of supplying the transients outlined above.

G. Test Procedure: Transients, Temperature, Voltage, and Humidity

1. Test A: Placement in Environmental Chamber and Check-Out of Hook-Up

   a. Place the test unit in the environmental chamber. Connect the test unit AC input circuit to a variable voltage power transformer, voltmeter, and transient generator. The transient generator must be connected to the AC input circuit at a point at least 25 feet from the AC power source and not over 10 feet from the input to the test unit.

   b. Connect test switches to the appropriate terminals to simulate the various features incorporated into the test unit. Place these switches in the proper position for desired operation.

   c. Verify the test hook-up. Adjust the variable-voltage power transformer to 120 VAC and apply power to the test unit. Verify that the test unit goes through its prescribed startup sequence and cycles properly in accordance with the operation determined by the positioning of test switches in item b.

      Upon the satisfactory completion and verification of the test hook-up, proceed with Test B.

2. Test B: Transient Tests (Power Service)

   a. Program the test unit to dwell. Verify the input voltage is 120 VAC.

   b. Set the transient generator to provide high-repetition noise transients as follows:

      (1) Amplitude: 300 Volts (+/-5 percent), both positive and negative polarity.

      (2) Peak Power: 2500 watts.

      (3) Repetition Rate: One pulse every other cycle moving uniformly over the full wave in order to sweep once every 3 seconds across 360 degrees of line cycle.

      (4) Pulse Rise Time: 1 microsecond.

      (5) Pulse Width: 10 microseconds.

c. Apply the transient generator output to the AC voltage input for at least 5 minutes. Repeat this test for at least two conditions of dwell for the test unit. The test unit must continue to dwell without malfunction.

d. Program the test unit to cycle through normal operations. Turn on the transient generator (output in accordance with item 2) for 10 minutes, during which time the test unit must continue to cycle without malfunction.

e. Set a transient generator to provide high-repetition noise transients as follows:

   (1) Amplitude: 300 Volts (+/-5 percent), both positive and negative polarity.

   (2) Source Impedance: Not less than 1000 ohms nominal impedance.

   (3) Repetition: One pulse per second for a minimum of five pulses per selected terminal.

   (4) Pulse Rise Time: 1 microsecond.

   (5) Pulse Width: 10 microseconds.

   Program the test unit to dwell. Verify the input voltage is 120 VAC.

f. Apply the transient generator (output in accordance with item 5) between logic ground and the connecting cable termination of selected Field I/O input/output terminals of the test unit.

   A representative sampling of selected input/output terminations must be tested. The test unit must continue to dwell without malfunction.

g. Program the test unit to cycle. Turn on the transient generator (output in accordance with item 5) and apply its output to the selected Field I/O input/output terminations. The test unit must continue to cycle without malfunction.

h. Reinstall protection and set a transient generator to provide low-repetition high-energy transients as follows:

   (1) Amplitude: 600 Volts (+/-5 percent), both positive and negative polarity.

   (2) Energy Discharge Source: Capacitor, oil-filled, 10 microfarads.

   (3) Repetition Rate: One discharge each 10 seconds.

   (4) Pulse Position: Random across 360 degrees of line cycle.

i. Program the test unit to dwell. Verify the input voltage is 120 VAC.

j. Discharge the oil-filled 10-microfarad capacitor ten times for each polarity across the AC voltage input. Repeat this test for at least two conditions of dwell. The test unit must continue to dwell without malfunction.

k. Program the test unit to cycle through normal operations. Discharge the capacitor ten times for each polarity while the test unit is cycling, during which time the test unit must continue to cycle without malfunction.

l. During the preceding transient tests, the test unit must continue its programmed functions.

   The test unit must not skip normal program intervals/steps or portions thereof when in normal operation; place false inputs or produce false outputs while in dwell; disrupt normal sequences in any manner; or change parameters.

m. Nondestructive Transient Immunity:

   (1) Turn off the AC power input to the test unit from the variable-voltage power source.

   (2) Apply the following high-energy transient to the AC voltage input terminals of the test unit (no other power connected to terminals):

      (a) Amplitude: 1000 V, both positive and negative polarity.

      (b) Peak Power Discharge: Capacitor, oil-filled, 15 microfarads.

      (c) Maximum Repetition Rate: Applied to the Cabinet Assembly once every 2 seconds for a maximum of three applications for each polarity.

   (3) Upon completion of the foregoing, apply 120 VAC to the test unit and verify that the test unit goes through its prescribed startup sequence and cycles properly in accordance with the programmed functions. The first operation of the over-current protective device during this test is not considered a failure of the test unit.

NOTE—Test C through G follow the profile indicated in Figure 1 to demonstrate the ability of the test unit to function reliably under stated conditions of temperature, voltage, and humidity.

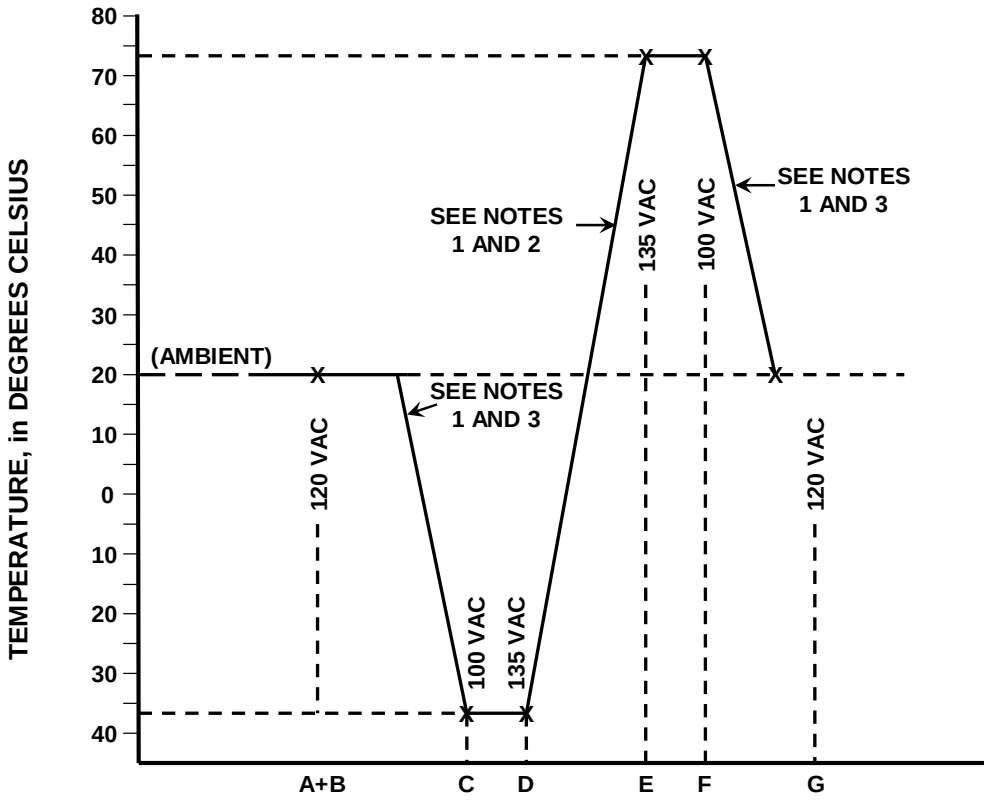

Figure 1
Test Profile

NOTES:

- The rate of change in temperature must not exceed 18 degrees C per hour
- Humidity controls must be set in conformance with the humidity given in Table 1 during the temperature change between Test D and Test E.
- If a change in both voltage and temperature are required for the next test, the voltage must be selected prior to the temperature change.

3. Test C—Low-Temperature Low-Voltage Tests

   a. Definition of Test Conditions

      (1) Environmental Chamber Door: Closed.

      (2) Temperature: -37 degrees C.

(3) Low Voltage: 100 VAC.

(4) Humidity Control: Off.

b. Test Procedure: While at room temperature, adjust the input voltage to 100 VAC and verify that the test unit is still operable.

(1) With the test unit cycling through normal operations, lower the test chamber to -37 degrees C at a rate not exceeding 18 degrees C per hour. Allow the test unit to cycle for a minimum of 5 hours at -37 degrees C with the humidity controls in the off position. Then operate the test switches as necessary to determine that all functions are operable.

(2) Remove power from the test unit for a minimum period of 5 hours. Upon restoration of power, the test unit must go through its prescribed startup sequence and then resume cycling.

(3) With the test unit at -37 degrees C and the input voltage at 100 VAC, evaluate the following items against the respective standards:

(a) Power Interruption Tests

On satisfactory completion of this test, proceed with Test D.

4. Test D—Low-Temperature High-Voltage Tests

a. Definition of Test Conditions

(1) Environmental Chamber Door: closed.

(2) Low Temperature: -37 degrees C.

(3) High Voltage: 135 VAC.

(4) Humidity Controls: Off.

b. Test Procedure: While at -37 degrees C and with humidity controls off, adjust the input voltage to 135 VAC and allow the test unit to cycle for 1 hour. Then operate the test switches as necessary to determine that all functions are operable.

c. With the test unit at -37 degrees C and the input voltage at 135 VAC (humidity controls off), evaluate the following items against the respective standards:

(a) Power Interruption Tests

On satisfactory completion of this test, proceed to Test E.

5. Test E—High-Temperature High-Voltage Tests

a. Definition of Test Conditions

(1) Environmental Chamber Door: Closed.

(2) High Temperature: +74 degrees C.

(3) High Voltage: 135 VAC.

(4) Humidity Controls: In accordance with the humidity given in Table 1.

b. Test Procedure—With the test unit cycling, raise the test chamber to +74 degrees C at a rate not to exceed 18 degrees C per hour. Verify the input voltage is 135 VAC.

c. Set the humidity controls to not exceed 95 percent relative humidity over the temperature range of +1.1 degrees C to +46 degrees C. When the temperature reaches +46 degrees C, readjust the humidity control to maintain constant absolute humidity; +42.7 degrees C wet bulb that results in the relative humidity shown in Table 1. Verify that the test unit continues to cycle satisfactory during the period of temperature increase and at established levels of relative humidity.

(1) Allow the test unit to cycle for a minimum of 15 hours at +74 degrees C and 18 percent relative humidity. Then operate the test switches as necessary to determine that all functions are operable.

(2) With the test unit at +74 degrees C and 18 percent relative humidity and the input voltage at 135 VAC, evaluate the following items against the respective standards:

(a) Power Interruption Tests

On satisfactory completion of this test, proceed to Test F.

6. Test F—High-Temperature Low-Voltage Tests

a. Definition of Test Conditions

(1) Environmental Chamber Door: Closed.

(2) High Temperature: +74 degrees C.

(3) Low Voltage: 100 VAC.

(4) Humidity Controls: 18 percent relative humidity and +42.7 degrees C wet bulb.

b. Test Procedure: Adjust the input voltage to 100 VAC and proceed to operate the test switches to determine that all functions are operable. With the test unit at +74 degrees C and 18 percent relative humidity, +42.7 degrees C wet bulb, and the input voltage at 100 VAC, evaluate the following items against the respective standards:

(a) Power Interruption Tests

On satisfactory completion of this test, proceed to Test G.

7. Test G—Test Termination

   a. Program the test unit to cycle.

   b. Adjust the input voltage to 120 VAC.

   c. Set the controls on the environmental chamber to return to room temperature, +20 degrees C (+/-5 degrees C), with the humidity controls in the off position. The rate of temperature change must not exceed 18 degrees C per hour.

   d. Verify the test unit continues to cycle through normal operations properly.

   e. Allow the test unit to stabilize at room temperature for 1 hour. Proceed to operate the test switches to determine that all functions are operable.

8. Test H—Appraisal of Equipment under Test

   a. A failure is defined as any occurrence that results in other than normal operation of the equipment. (See sub-section item b. below for details.) If a failure occurs, the test unit must be repaired or components replaced, and the test during which failure occurred must be restarted from its beginning.

   b. The test unit is considered to have failed if any of the following occur:

      (1) If the test unit skips normal program intervals/steps or portions thereof when in normal operation, places false inputs, presents false outputs, exhibits disruption of normal sequence of operations, or produces changes in parameters beyond specified tolerances, or

      (2) If the test unit fails to satisfy the requirements of Tests A to G, inclusive.

   c. An analysis of the failure must be performed and corrective action taken before the test unit is retested in accordance with this standard. The analysis must outline what action was taken to preclude additional failures during the tests.

   d. When the number of failures exceeds two, it must be considered that the test unit fails to meet these standards. The test unit may be completely retested after analysis of the failure and necessary repairs have been made in accordance with item c.

   e. Upon completion of the tests, visually inspect the test unit. If material changes are observed which will adversely affect the life of the test unit, the cause and conditions must be corrected before making further tests.

f. Upon satisfactory completion of all of the tests described, test the unit in accordance with Vibration Test.

H. Vibration Test.

1. Purpose of Test. This test is intended to duplicate vibrations encountered by the test unit (individual major components) when installed at its field location.

   Fasten the test unit securely to the vibration test table prior to the start of the test.

2. Test Equipment Requirements.

   a. Vibration table with adequate table surface area to permit placement of the test unit.

   b. Vibration test consists of:

      (1) Vibration in each of three mutually perpendicular planes.

      (2) Adjustment of frequency of vibration over the range from 5 hertz to 30 hertz.

      (3) Adjustment of test table excursion (double amplitude displacement) to maintain a ‘g’ value, measured at the test table, of 0.5g; as determined by the following formula:

         $g = 0.0511df^2$

         Where:

         d = excursion in inches

         f = frequency in hertz

3. Resonant Search

   a. With the test unit securely fastened to the test table, set the test table for a double amplitude displacement of 0.015 inch.

   b. Cycle the test table over a search range from 5 hertz to 30 hertz and back within a period of 12.5 minutes.

   c. Conduct the resonant frequency search in each of the three mutually perpendicular planes.

   d. Note and record the resonant frequency determined from each plane.

      (1) In the event of more than on resonant frequency in a given plane, record the most severe resonance.

(2) If resonant frequencies appear equally severe, record each resonant frequency.

(3) If no resonant frequency occurs for a given plane within the prescribed range, 30 hertz must be recorded.

4. Endurance Test

a. Vibrate the test unit in each plane at its resonant frequency for a period of 1 hour at amplitude resulting in 0.5g acceleration.

b. When more than one resonant frequency has been recorded, the test period of 1 hour must be divided equally between the resonant frequencies.

c. The total time of the endurance test must be limited to 3 hours, 1 hour in each of three mutually perpendicular planes.

5. Disposition of Equipment under Test

a. Examine the test unit to determine that no physical damage has resulted from the vibration tests.

b. Check the test unit to determine that it is functionally operable in all modes of its prescribed operation.

c. The test unit may be removed from the test table. Upon satisfactory completion of the vibration test, proceed with the shock (impact) test.

I. Shock (Impact) Test.

1. Purpose of Test. The purpose of this test is to determine that the test unit is capable of withstanding the shock (impact) to which it may reasonably be subjected during handling and transportation in the process of installation, repair, and replacement. It is to be noted that the test unit is not, at this time, in its shipping carton.

Fasten the test unit firmly to the specimen table. In each of its three planes the test, drop the unit from a calibrated height to result in a shock force of 10g.

2. Test Equipment Requirements.

a. Shock (impact) test fixture equivalent to that suggested by the simplified sketch shown in Figure 2.

b. The test table must have a surface area sufficient to accommodate the test unit.

c. Calibrate the test table and the items tested as indicated. This shock test defines the test shock to be 10g (+/-1g).

(1) Measure calibration of the test equipment for these shock tests by three accelerometers having fixed shock settings of 9g, 10g, and 11g. They must be Inertia Switch Incorporated ST-355, or the equivalent. Attach these devices rigidly to the test table.

(2) Calibration of the fixture for each item to be tested is as follows:

(a) Place a dummy load weighing within 10 percent of the test unit on the table.

(b) Reset the three accelerometers and drop the test table from a measured height.

(c) Observe that the accelerometers indicate the following:

- Activate the 9g accelerometer.
- The 10g unit may or may not be actuated.
- The 11g unit must not be actuated.

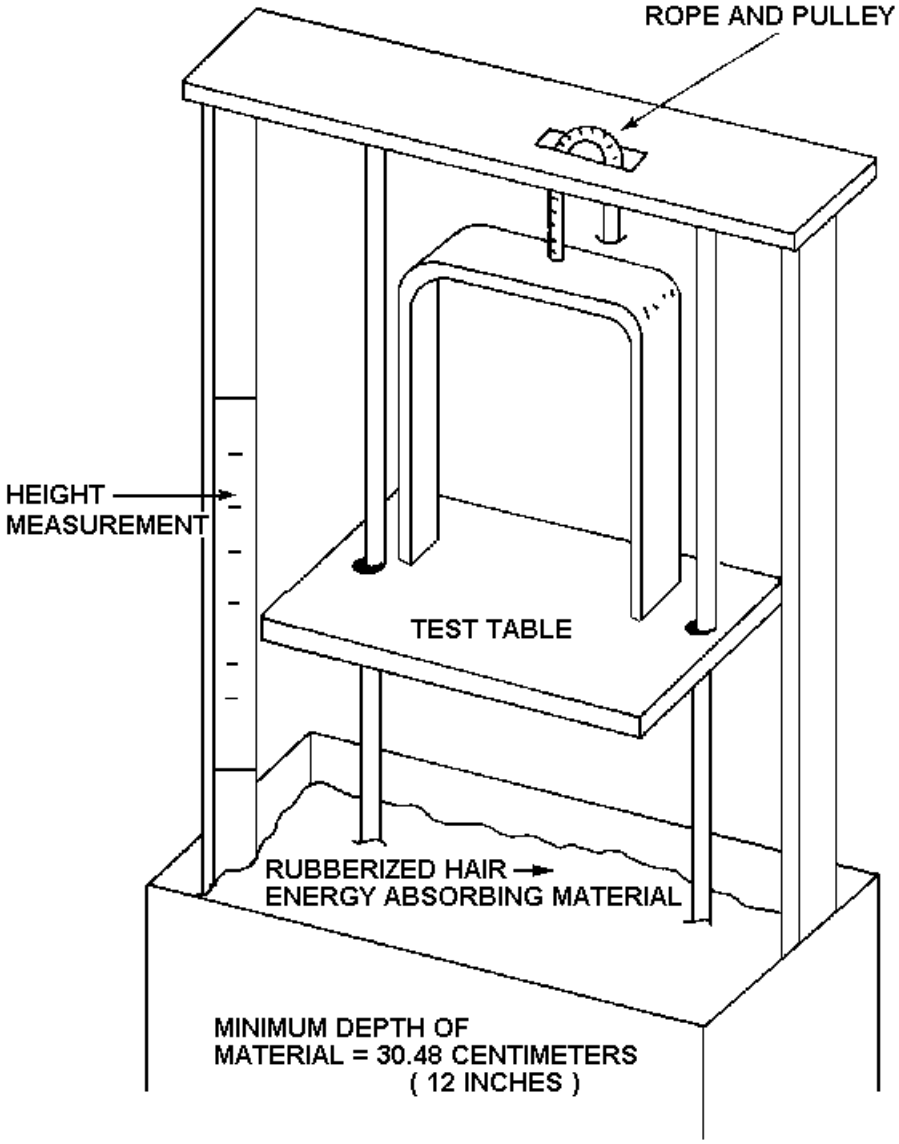

Figure 2
Shock Test Fixture

(3) Repeat calibration test (a) and (b) adjusting the height of the drop until, on ten successive drops, the following occurs:

(a) The 9g unit is actuated ten times.

(b) The 10g unit is actuated between four to eight times.

(c) The 11g unit is not actuated on any of the ten drops.

3. Test Procedure.

a. The calibration height of the drop for the particular item under test as determined in Test Equipment Requirements must be used in this procedure.

b. Secure the test unit to the test table surface so that the test unit rests on one of its three mutually perpendicular planes.

c. Raise the test table to the calibrated height.

d. Release the test table from the calibrated height, allowing a free fall into the box of energy absorbing material below.

e. Repeat the drop test for each of the remaining two mutually perpendicular planes, using the same calibrated height for each drop test of the same test unit.

f. The observations of the accelerometer for the three tests of the test item are:

(1) The 9g unit is actuated for all three tests. (Repeat the calibration if the unit is not actuated.)

(2) The 10g unit may or may not be actuated in these tests.

(3) The 11g unit is not actuated on any drop. (If the unit is actuated, repeat the calibration only if the test unit has suffered damage.)

4. Disposition of Test Unit.

a. Check the test unit for any physical damage resulting from the drop tests.

b. Check the test unit to determine that it is functionally operable in all modes of its prescribed operation.

c. Satisfactory completion of all environmental tests, including the shock (impact) is required.

J. Power Interruption Test Procedures. Conduct the following power interruption tests at low input voltage (100 VAC) and high input voltage (135 VAC) at -37 degrees C, and +74 degrees C.

1. Short Power Interruption. While the Test Unit is cycling through normal operations, remove the input voltage for a period of 475 milliseconds. Upon restoration of the input voltage, check to insure that the Test Unit continues normal operation as though no power interruption has occurred. Repeat this test three times.

2. Voltage Variation. All circuits of the Test Unit must be subjected to slowly varying line voltage during which the Test Unit must be subjected to line voltage that is slowly lowered from a nominal 120 VAC line voltage to 0 VAC at a rate of not greater than 2 Volts per second. The line voltage must

then be slowly raised to 100 VAC at which point the Test Unit must resume normal operation without operator intervention. Perform this test at both -37 degrees C and +74 degrees C, at a nominal 120 VAC line voltage. Repeat this test three times.

3. Rapid Power Interruption. Subject the Test Unit to rapid power interruption testing of the form that the power is off for 350 milliseconds and on for 650 milliseconds for a period of 2 minutes. Perform power interruption through electromechanical contacts of an appropriate size for the load. During this testing, the controller must function normally and continue normal sequencing (operation) at the conclusion of the test. This test must be performed at both -37 degrees C and +74 degrees C, at a nominal 120 VAC line voltage. Repeat this test three times.

2.07 TYPE 2070 CONTROLLER UNIT

A. General.

1. Module Descriptions. The Controller Unit is composed of the Type 2070 Unit CHASSIS, along with other modules and assemblies. The following is a list of Type 2070 versions, their interface rolls and composition:

Unit Version	Description
Type 2070V Unit	Provides directly driven VME and mates to 170 & ITS cabinets. It consists of: Unit CHASSIS, 2070-1A TWO BOARD CPU, 2070-2A (2B if ITS CABINET) FI/O, 2070-3A FRONT PANEL, 2070-4A POWER SUPPLY, and 2070-5 VME CAGE ASSEMBLY.
Type 2070L Unit	LITE Unit mates to the 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1B CPU, 2070-2A (2B if ITS CABINET), FI/O, 2070-3B FRONT PANEL and 2070-4A or B POWER SUPPLY.
Type 2070LS Unit	LITE unit mates to ITS serial cabinets only. It consists of: UNIT CHASSIS, 2070-1B CPU, 2070-2B FI/O, 2070-3C FRONT PANEL and 2070-4 A or B POWER SUPPLY.

2. Unit Configuration. The Type 2070 Controller Unit Version defines the module composition to be delivered as follows:

No.	Item	Description	Composition		
			2070V Unit	2070L Unit	2070LS Unit
1	---	UNIT CHASSIS	Y	Y	Y
2	TYPE 2070-1A	CPU MODULE, MULTIPLE BOARD-VME	Y	---	---
3	TYPE 2070-1B	CPU MODULE, SINGLE BOARD- SERIAL HUB	---	Y	Y
4	TYPE 2070-2A	FIELD I/O MODULE (FI/O for 170 Cabinet)	Y	Y user selection Y	---
5	TYPE 2070-2B	FIELD I/O MODULE (ITS & NEMA Cabinets)	---		Y
6	TYPE 2070-3A	FRONT PANEL MODULE (FP), DISPLAY A	Y	---	---
7	TYPE 2070-3B	FRONT PANEL MODULE (FP), DISPLAY B	---	Y	---
8	TYPE 2070-3C	FRONT PANEL MODULE (FP), BLANK	---	---	Y
9	TYPE 2070-4A	POWER SUPPLY MODULE, 10 AMP	Y	Y user selection Y	Y user selection Y
10	TYPE 2070-4B	POWER SUPPLY MODULE, 3.5 AMP	---		
11	TYPE 2070-5A	VME CAGE ASSEMBLY	Y	---	---

2070V UNIT	1+2+4+6+9+11	Provides directly driven VME and mates to 170 and ITS cabinets
2070L UNIT	1+3+(4 or 5)+7+(9 or 10)	LITE Unit mated to 170 and ITS cabinets
2070LC UNIT	1+3+5+8+(9 or 10)	LITE unit mates to ITS cabinets only

a. The communications and option modules/assemblies must be called out separately from the unit version. The composition weight must not exceed 25 pounds.

3. Metalwork. The CHASSIS Top and Bottom, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Power Supply Enclosure, and Front Panel must be made of 63-gauge minimum aluminum sheet. The CHASSIS Side panels must be 80-gauge minimum sheet.

4. Power Fail and Power Restoration Operation. It is noted that the Power Failure Power Restoration operations of this unit are specific to the requirements of the user. All associated modules are to comply to said operations.

5. Power Limitations. 2070 UNIT module / assembly power limitations are as follows:

Types	+5VDC	+12VDC ISO	+12VDC ser	-12 VDC ser
MCB	750 milliamperes	-----	-----	-----
TRANS BD	750 milliamperes	-----	-----	-----
2070-1B CPU	1.0 amperes	250mA	-----	-----
2070-1C	1.0 amperes	250mA	-----	-----
2070-2A FI/O	250 milliamperes	750 milliamperes	-----	-----
2070-2B FI/O	250 milliamperes	500 milliamperes	-----	-----
2070-3A&B FPA	500 milliamperes	-----	50 milliamperes	50 milliamperes
2070-3C FPA	100 milliamperes	-----	50 milliamperes	50 milliamperes
2070-5 VME Cage	5.0 amperes	-----	200 milliamperes	200 milliamperes
2070-6 All Comm	500 milliamperes	-----	100 milliamperes	100 milliamperes
2070-7 All Comm	250 milliamperes	-----	50 milliamperes	50 milliamperes

6. EIA-485 Communications Circuitry. All circuitry associated with the EIA-485 Communications links must be capable of reliably passing a minimum of 1.0 megabits per second. Isolation circuitry must be by opto- or capacitive-coupled isolation technologies.

7. EIA-485 Line Drivers/Receivers. Through hole EIA-485 Line Drivers/Receivers, when used, must be socket mounted. Surface mounted drivers/receiver must be acceptable. EIA-485 Line Drivers/Receivers must not draw more than 35 milliamperes in active state and 20 milliamperes in inactive state per channel. A 100-Ohm Termination Resistor must be

provided across each Differential Line Receiver Input. The Motherboard's control signals (e.g., SP1-RTS) must be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals must be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

8. Sockets. Sockets for devices (called out to be socket mounted) must be "xx" pin AUGAT 500/800 series AG10DPC or equal.

9. SDLC. SP5and SP3 SDLC frame address assignments (Command/Response) are as follows:

		SP5	*SP3*
CPU 2070-1	=	"19"	"19"
FI/O 2070-2A & 8	=	"20"	"Not Applicable"
CPU Broadcast to all	=	"255"	"255"

All other addresses are reserved by this standard. The SDLC response frame address must be the same address as the Command frame it receives.

B. Type 2070-1 CPU Module.

1. Type 2070-1A Configuration. The TYPE 2070-1A CPU consists of the Main Controller Board, Transition Board, Board Interface Harness, and CPU Module Software.

2. Type 2070-1B Configuration. The TYPE 2070-1B CPU must be a single board module meeting the 2X WIDE board requirements. The module must be furnished normally resident in MOTHERBOARD Slot A5. The module must meet all the requirements listed under this section and Details except for the following:

   a. The VME software and hardware bus requirement does not apply nor do the MCB and Board Interface Harness physical requirements.

   b. A Dual SCC Device (asynch/synch) and associated circuitry must be furnished to provide two additional system serial ports. The Dual SCC1 must be assigned to the System Serial Port SP1 meeting all requirements called out for SP1. The Dual SCC2 must be assigned as System Serial Port SP8. The SP8 and associated circuitry must interface with the MC68360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. The SP8 must meet all SP2 Port

requirements including EIA 485 Drivers / receivers and synchronous data rate of 614.4 kilobits per second.

c. The 68360 SCC1 must be reassigned to ETHERNET (ENET) Network meeting ETHERNET 10 MBPS IEEE 802.3 (TP) 10 BASE T Standard Requirements, both hardware and software. The four network lines must be used to route ETHERNET across the MOTHERBOARD to the "A" Connectors. DC Grounding plane around the network connectors and lines to be provided. Network Lines must be assigned as: Network 1 = ENET TX+, Network 2 = ENET TX-, Network 3= ENET RX+, and Network 4 = ENET RX-. In addition, the conditioned ETHERNET must be brought out on RJ 45 C14S Connector mounted on the CPU-1B Front Panel. Four LEDs labeled "TX, RX, TX Collision and TX Status" must be mounted on the front panel signifying ETHERNET operational conditions.

d. The 2070-1B CPU must not draw more than 1.00 Amperes of +5VDC and 250 milliamperes of ISO+12 VDC.

3. Type 2070 – 1C Configuration. The TYPE 2070-1C CPU must be a single board module meeting the 2X WIDE board requirements. The module must be furnished normally resident in MOTHERBOARD Slot A5. The module must meet all the requirements listed under the 2070-1B section of this standard, with the following additions:

a. Engine Board. The TYPE 2070-1C CPU must use an Engine Board compliant to the AASHTO/ITE Next Generation ATC Standard. The Engine Board must be used for execution of the application software. No other microprocessor or memory of the 2070-1C CPU to be used for execution of the application software.

b. Ethernet Ports. The second ETHERNET port of the Engine Board must be brought out on an RJ 45 C15S Connector mounted on the 2070-1C front panel. The front panel LED indicators for the two Ethernet ports must conform to the AASHTO/ITE Next Generation ATC Standard.

c. Universal Serial Bus (USB). The TYPE 2070-1C CPU must include a USB port compliant to the AASHTO/ITE Next Generation ATC Standard, and brought out from the Engine Board to a USB C16S Connector mounted on the 2070-1C front panel.

d. Host Module Identification. The TYPE 2070-1C CPU must implement the host module identification using the Engine Board SPI serial port, compliant to the AASHTO/ITE Next Generation ATC Standard.

4. Main Controller Board (MCB).

a. General. The MCB must be a 3U VME bus compliant board and contain a system controller, an A24-D16 interface, a Master & Slave bus

interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester, a system clock driver, and BTO (64).

b. Controller. The CONTROLLER Device must be a Motorola MC68360 or equal, clocked at 24.576 MHz minimum. The Fast IRQ Service System is reserved for CITY OF HOUSTON use only. The Interrupts must be configured as follows:

Level 7 -	VMEbus IRQ7	
Level 6 -	VMEbus IRQ6	ACFAIL
Level 5 -	VMEbus IRQ5	CPU Module Counters / Timers, LINESYNC (auto vectored), Serial Interface Interrupts
Level 4 -	VMEbus IRQ4	
Level 3 -	VMEbus IRQ3	
Level 2 -	VMEbus IRQ2	
Level 1 -	VMEbus IRQ1	

c. Memory Address Organization.

8000 0000 - 80FF FFFF STANDARD

9000 0000 - 9000 FFFF SHORT

(1) 16 megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) allocated on an even boundary. The SRAM and FLASH memories must be accessed through the OS-9 Operating System's File Manager, or approved equivalent. The address of each memory block must be specified by the manufacturer and provided with the documentation.

(2) When the incoming +5 VDC falls below its operating level, the SRAM must drop to its standby state; and the SRAM and TOD Clock shift to the +5 VDC Standby Power. An on-board circuit will sense the +5 VDC Standby Power and shift to an On-board CPU Power Source. When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry will shift from standby power to incoming +5 VDC.

d. RAM Memory. Provide a minimum of 8 megabytes of DRAM Memory, organized in 32-bit words. A minimum of 1 megabyte of SRAM is required, of which 512 KiloBytes minimum must be available for City of Houston use as a RAM drive (R0). The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device must not exceed 80

nanoseconds and be less as required to fulfill zero wait state RAM device write access under all operational conditions.

e. FLASH Memory. Provide a minimum of 8 MB of FLASH memory, organized in 16- or 32- bit words. The MCB must be equipped with all necessary circuitry for writing to the FLASH memory under program control. No more than 2 MB of FLASH Memory to be used for the Boot Image (List) and a minimum of 6 MB be available for CITY OF HOUSTON use. The 2 MB of FLASH Memory must be reserved for the Boot Image only. Flash memory must have a minimum rated capacity of 100,000 read/write cycles and be industrial grade or better.

f. Time-of-Day Clock. Provide a software settable hardware Time-of-Day (TOD) clock. It must maintain an accuracy of +/-1 minute per 30 days at 25 degrees C (77 degrees F) under on-board standby power. The clock must be aligned to a minimum fractional second resolution of 10 milliseconds and track seconds, minutes, hours, day of month, month, and year.

g. CPU Reset. Provide a software-driven CPU RESET signal (Active LOW) to reset other controller systems. The signal output must be driver capable of sinking 30 milliamperes at 30 VDC. Execution of the program module “CPURESET” in the boot image must assert the CPU RESET signal once.

h. CPU Activity Indicator. Provide an open-collector output, capable of sinking 30 milliamperes at 30 VDC, to drive the Front Panel Assembly CPU Activity LED INDICATOR.

i. Tick Timer. The OS-9 Operating System TICK Timer must be derived from each transition of LINESYNC with a tick rate of 120 ticks per second.

j. SRAM and TOD Holdup. The SRAM and TOD Clock Circuitry, under Standby mode, must draw no more than 8 microamperes at 2.5 VDC and 35 degrees C. Supply an On-board Capacitor to hold up SRAM and TOD or a minimum of 7 days.

5. Transition Board. Provide a TRANSITION Board (TB) to transfer serial communication and control signals between the MCB and the Interface Master-board. Said signal and communication lines must be driven/received off and on the module compliant to EIA- 485. The Transition Board must provide a 1 KiloOhm pull-up resistor for the A2 & A3 installed lines. If the DC Ground is not present (slot not occupied) at the CPU EIA-485 line drivers/receivers, the drivers/receivers must be disabled (inactive).

6. Shielded Interface Harness. Provide a SHIELDED INTERFACE HARNESS that includes MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors. A minimum of 25 mm of

slack must be provided. No power to be routed through the harness. The harness must be 100% covered by an aluminum mylar foil and an extruded black 0.8 mm PVC jacket or equal.

7. DataKey. Provide a DATAKEY Keyceptacle™ (KC4210, KC4210PCB or equal) mounted on the CPU module front panel (or the Transition Board of Type 1A). Power must not be applied to the receptacle if the key is not present.

   The Manufacturer must supply a 2-megabyte Memory Size Datakey (SFK2Mb or equal) with each MODEL 1A TB (Transition Board) or 1B CPU module unless specified otherwise. The Datakey must be temperature rated for –40 to +80 degrees C operation, be black in color, and be initialized to the format and default values defined below.

   When programmed, the memory on the key of header version 1 must be organized as follows:

Bytes	Description	Default Values
1-2	16 bit Frame Check Sequence (FCS) calculated as defined in clause 4.6.2 of ISO/IEC 3309. This FCS is calculated across bytes 3-64	
3	Key Type	See table below
4	Header Version	1
5-8	Latitude	0.0
9-12	Longitude	0.0
13-14	Controller ID	0xFFFF
15-16	Communication drop number	0xFFFF
17-20	IP Address	10.20.70.51
21-24	Subnet Mask	255.255.255.0
25-28	Default Gateway	10.20.70.254
29	Startup Override	0xFF
30-64	Reserved for City of Houston use	All bytes set to 0xFF
65 to End	User Data	All bytes set to 0xFF

   When programmed, Byte 3 of the header must contain the Key Type value as defined in the following table:

Key Type	Model No.	Memory Size	Sector Size
1	DK1000	1 KiloByte	1 Byte
2	LCK16000	16 KiloBytes	1 Byte
3	SFK2Mb	2 megabytes	64 KiloBytes
4	TBD	4 megabytes	64 KiloBytes

Key Type	Model No.	Memory Size	Sector Size
5	TBD	8 megabytes	64 KiloBytes

The data format in the CPU Datakey header for the Latitude and Longitude fields must comply with IEEE/ANSI 754-1985 STD. All the other fields follow a Big Endian Format as implemented by Motorola CPUs.

The Startup Override byte may be used to override the default controller startup procedure.

8. CPU Module Software. The following must be supplied:
   - Operating System
   - Drivers and Descriptors
   - Application Kernel
   - Deliverables
   - Error Handler

   a. Operating System. The CPU Module must be supplied with Radisys/Microware OS-9 Version 3.2, or later, with kernel edition #372 or later. The following modules must be included:
      - Embedded OS-9 Real Time Kernel
      - Sequential Character File Manager (SCF)
      - Stacked Protocol File Manager (SPF)
      - Pipe File Manager (PIPEMAN)
      - Random Block File Manager (RBF)
      - C Shared Library (CSL)

      Boot Image must include the following utility modules:

Break	Date	Deiniz	Devs	Free	Copy
Dir	Tmode	Edt	List	Load	Deldir
Dump	Del	Ident	Iniz	Irqs	Events
Echo	Format	Dcheck	Login	Link	Kermit
Tsmon	Mdir	Mfree	Pd	Makdir	Save
Attr	Rename	Procs	Unlink	Sleep	Xmode
Shell	Build	Setime	Merge	grep	

   b. Drivers and Descriptors.

      (1) Supplied modules must be re-entrant, address independent, and not contain self-modifying code.

      Device drivers which require extensions to the standard OS-9 libraries must use the _os_getstat() and _os_setstat() functions.

```
#define SS_2070     0x2070

error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);

error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);

typedef struct

{

    u_int32 code;

    u_int32 param1;

    union

    {

        u_int32 param;

        void    *pointer;

    } param2;

} PB2070, *pb;
```

The following subcodes for use with PB2070.code are also defined:

```
#define GS2070_Status       0x1C
#define SS2070_SSig         0x1A
#define SS2070_IFC          0x22
#define SS2070_OFC          0x23
#define SS2070_Timer_Sig    0x1000
#define SS2070_Timer_Cyc    0x1001
#define SS2070_Timer_Start  0x1002
#define SS2070_Timer_Stop   0x1003
#define SS2070_Timer_Reset  0x1004
```

Note: When PB2070.param2.pointer is used, PB2070.param1 to be loaded with the size of what PB2070.param2.pointer is referencing. When calling _os_getstat() or _os_setstat(), all reserved or unused parameters and fields in PB2070 to be loaded with 0 (zero).

(2) Drivers must be provided to access the FLASH, SRAM, and DRAM memories. The following descriptors must apply:

/f0	FLASH drive	non-volatile, writeable
/dd	FLASH drive	OS-9 default device for /f0
/f0wp	FLASH Drive	as /f0 but, write protection
/f0fmt	FLASH Drive	as /f0 except format enabled
/r0	SRAM Drive	non-volatile ramdisk
/r0fmt	SRAM Drive	as /r0 but format enabled

/r2	DRAM Drive	volatile 1 MB ramdisk, not automatically initialized

(3) A driver to handle each of the four internal timers under the OS-9 Kernel must be provided. Provide access to the MC68360 internal timers through the following device descriptors:

(a) Descriptor names for each timer:

timer1 = access to MC68360's internal timer #1
timer2 = access to MC68360's internal timer #2
timer3 = access to MC68360's internal timer #3
timer4 = access to MC68360's internal timer #4
timer12 = access to MC68360's internal timer #1 & #2 (cascaded)
timer34 = access to MC68360's internal timer #3 & #4 (cascaded)

(b) Timer Standard OS-9 Function Calls:

error_code _os_open (char *timer_desc_name, path_id *path);

error_code _os_read (path_id path, void *timer_value, u_int32 *size);

Note: Prior to calling _os_read(), size must be loaded with the value 4 and timer value must be pointed to a u_int32. _os_read() must read the current timer value and load it into timer_value as μS x 100.

error_code _os_close (path_id path);

(c) Timer Extension to Standard OS-9 Function Calls:

error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);

The timer drivers must support the following modes using the SS_2070 _os_setstat() option code and a custom parameter block structure:

- Send signal after specified time interval. Sets timer to zero and schedules individual one-shot signal.

  pb→code = SS2070_Timer_Sig (0x1000); /* request for one-shot signal */

  pb.param1 = signal; /* signal code to send (0 = do not send a signal and cancel any pending signals) */”

pb→param2.param = period; /* timer period in microseconds x 100 */

- Send recurring periodic signal. Sets timer to zero and schedules repeating periodic signal.

  pb→code = SS2070_Timer_Cyc (0x1001); /* request for periodic signal */

  pb.param1 = signal; /* signal code to send (0 = do not send a signal and cancel any pending signals) */"

  pb→param2.param = period; /* timer period in microseconds x 100 */

- Start timer. Start the timer if stopped. Timer will free run in a periodic mode, starting at the current timer value as its initial value and timer's maximum allowable time as its timer period (6.5535 seconds for timers 1-4 and 429496.7295 seconds for timers 12 and 34). Timer will not send a signal and any pending signals will be cancelled. Timer mode will be SS2070_Timer_Start. pb.code = SS2070_Timer_Start (0x1002); /* start timer if stopped */"
- Stop timer. Leaves current value in timer. Cancels any pending signals.

  pb→code = SS2070_Timer_Stop (0x1003); /* stop timer if running */
- Reset timer. Stops timer if running, resets timer value to zero, and cancels any pending signals.

  pb→code = SS2070_Timer_Reset (0x1004);/* reset timer (stop and zero) */

(d) Timer Extension to Standard OS-9 Function Calls:

error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);

The timer driver will support the following function using the SS_2070 _os_getstat() option code and custom parameter block structure:

- Retrieve current timer configuration.

```
typedef struct
{
    u_int32 value;
    u_int32 mode;
```

```
        u_int32 signal;
        u_int32 period;
    } Timer_status;

    pb→code = GS2070_Status  (0x1C)      /* Request timer
    status data */
    pb→param1 = sizeof(Timer_status)
    pb→param2.pointer = Timer_status*
```

Status data must be returned in the structure pointed to by pb→param2.pointer as follows:

```
pb→param2.pointer→value      /* current timer value in µS x 100 */

pb→param2.pointer→mode       /* SS2070_Timer_Sig if one-shot signal
                                pending,
                                SS2070_Timer_Cyc if periodic signal pending,
                                SS2070_Timer_Start if free running,
                                SS2070_Timer_Stop if not active */

pb→param2.pointer→signal     /* signal code pending if
                                SS2070_Timer_Sig or
                                SS2070_Timer_Cyc, 0 otherwise */

pb→param2.pointer→period     /* timer period in microseconds x 100 if
                                SS2070_Timer_Sig or
                                SS2070_Timer_Cyc, 0 otherwise */
```

(e) All timer periods are specified in units of hundreds of microseconds, i.e. a timer period of 7 = 700 microseconds. The minimum allowed timer period must be 500 microseconds. The maximum timer period for timers 1-4 must be 6.5535 seconds (0xFFFF). The maximum timer period for timer12 and timer34 must be 429496.7295 seconds (0xFFFFFFFF). The driver must return error E$Param from _os_setstat() if the requested timer period is outside the allowable range.

(4) Access and control to the CPU Datakey must be provided through the following descriptor name and OS-9 functions:

<u>Descriptor Name</u>

datakey = access to the CPU Datakey

<u>Function Calls</u>

```
error_code _os_open (char *datakey_desc_name, path_id *path);

error_code _os_close (path_id path);
```

error_code _os_read (path_id path, void *data_buffer, u_int32 *data_size);

error_code _os_write (path_id path, void *control, u_int32 *data_size);

error_code _os_seek(path_id path,u_int32 position); sets read / write offset

error_code = _os_ss_erase(path_id path, u_int32 num_sec_erase); /*erases sector(s) if pointer is on a block boundary, returns E$PARAM error if not on a boundary */"

error_code = _os_gs_pos(path_id path,u_int32 *position); /* gets current file pointer position */

error_code = _os_gs_size(path_id path, u_int32 *size); /* gets current datakey size */"

Error Codes Returned by Function Calls

E$NotRdy if datakey is not inserted
E$Seek if Offset plus *data_size is beyond end of CPU Datakey.
E$EOF if upon read or write, the last byte of CPU Datakey has previously been processed."

Note: Use of SCF to implement the Datakey driver is not allowed.

(5) The asynchronous serial communications device drivers must support the six flow control modes (FCM#) described below:

FCM# Description

(0) No Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed. This is the default mode. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode (FCM# 1).

(1) Manual Flow Control Mode: The driver transmits data regardless of the state of CTS. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.

(2) Auto-CTS Flow Control Mode: The driver transmits data only when CTS is externally asserted. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.

(3) Auto-RTS Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If the user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.

(4) Fully Automatic Flow Control Mode: The driver transmits data only when CTS is externally asserted. Upon a write command, the driver asserts RTS and waits for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.

(5) Dynamic Flow Control Mode: The driver transmits data only when CTS is externally asserted. The driver controls RTS based on the status of its receiving buffer. The driver asserts RTS continuously as long as its receiving buffer has sufficient capacity to store incoming data. If the receiving buffer approaches full, the driver de-asserts RTS until enough data has been read from the buffer to create sufficient receive capacity.

(a) The serial device driver must be able to set user options via _os_setstat() and return status via _os_getstat(). To support legacy application programs, the device driver must also be able to set user options via _os_ss_size() and to return status via _os_gs_size():

```
error_code_os_setstat(path_id path, SS_2070, void *pb);
error_code_os_getstat(path_id path, SS_2070, void *pb);
error_code_os_ss_size(path_id path, u_int32 size);
error_code_os_gs_size(path_id path, u_int32 *size);
```

Note: The preferred method of accessing serial device drivers is through _os_setstat() and _os_getstat(). The _os_ss_size() and _os_gs_size() interface may not be required by future versions of this specification and is therefore not recommended for new development.

The option subcodes to be passed in pb→code and the data to be contained in pb→param1 are defined as follows. pb→param2 is unused here and should be set to 0 (zero). For _os_ss_size() and _os_gs_size(), the size argument is the same format as pb→param1.

(b) The supported _os_setstat() / _os_ss_size() options must be as follows.

- Subcode passed in pb→code is SS2070_OFC (0x23). Data passed in pb→param1 is defined as follows:

Bits	Description
31-24	Auto RTS turn-off extension in number of characters (range:0-255, 0=default).
23-14	Reserved for future use.
13	Inhibit return of error E$Write from _os_write() when transmit buffer full in FCM# 2, 4, 5 (default=0, 0=error, 1=block)
12	Inhibit variable SCC MRBLR (default =0; 0=NO; 1=inhibit).
11	Inhibit SCC TODR (default=0; 0=NO; 1=inhibit).
10-8	Flow Control Mode Number (FCM#) (range:0-5).
7-0	Subcode SS2070_OFC (0x23).

Variable MRBLR (68360 SCC)

To reduce the IRQ handler overhead, the 68360 SCC driver must use variable MRBLR as follows. If SS2070_OFC bit 12 is set to 1, the MRBLR must be fixed at 16 for all baud rates. Variable MRBLR is not required for SP1 or SP8 on the 2070-1B CPU Module.

Baud Rate	MRBLR Setting
1200	1
2400	2
4800	4
9600	8
19200 & Higher	16

TODR (68360 SCC only)

TODR requests processing a new TX buffer immediately. To reduce impact on other serial channel operations, SS2070_OFC bit 11 may be set to 1 to prevent assertion of TODR. TODR is not required for SP1 or SP8 on the 2070-1B CPU Module.

- Subcode passed in pb→code is SS2070_IFC (0x22). Data passed in pb→param1 is defined as follows:

Bits	Description
31-11	Reserved for Future Use.
10	DCD must be asserted to receive data (default=0; 0=NO; 1=YES).
9-8	Reserved for Future Use.
7-0	Subcode = SS2070_IFC (0x22).

- Subcode passed in pb→code is SS2070_SSig (0x1A).

1. If CTS is currently negated and bits 16 – 31 are not all 0:

   Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal as soon as CTS is asserted.

   Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot signal immediately.

2. If CTS is currently asserted and bits 16 – 31 are not all 0:

   Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal immediately.

   Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a signal one-shot as soon as CTS is negated.

3. If both bits 11 and 12 of the SS2070_SSig parameter block are set, and bits 16 – 31 are not all 0:

   The controller will send a one-shot signal upon the next change of CTS state.

Data passed in pb→param1 is defined as follows:

Bits	*Description*
31-16	A signal number to be sent to calling process when the state of an input changes.

Bits	*Description*
15-13	Reserved for Future Use.
12	Send signal when CTS is de-asserted.
11	Send signal when CTS is asserted.
10-8	Reserved for Future Use.
7-0	Subcode = SS2070_SSig (0x1A).

(c) The supported _os_getstat()_ / _os_gs_size() options must be as follows.

- Subcode passed in pb→code is GS2070_Status (0x1C). Data returned in pb→param1 is defined as follows:

its	Description
1-16	Current unfilled transmit buffer character count of the serial device driver.
5-11	Reserved for Future Use.
0-8	Current Flow Control Mode Number (FCM#).
	Reserved for Future Use.
	Overrun error –0=no error; 1=error has occur since last GS2070_Status call.
	Frame error –0=no error; 1=error has occur since last GS2070_Status call.
	Parity error –0=no error; 1=error has occur since last GS2070_Status call.
-2	Reserved for Future Use.
	DCD state –0=de-asserted; 1=asserted.
	CTS state –0=de-asserted; 1=asserted.

(6) Device drivers compliant with the OS-9 SCFMAN must be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names must be as follows:

led = access to CPU Activity LED Indicator

dstclock = access to Daylight Savings Time Clock correction
The standard OS-9 SCFMAN library calls and their functions are as follows:

error_code _os_open (char *desc_name, path_id *path); //open descriptor for command

error_code _os_close (path_id path); //close descriptor

error_code _os_write (path_id path, void *value, u_int32 *data_size); //set value of function

*value = 1, turn on LED or enable DST correction (default)
*value = 0, turn off LED or disable DST correction
set u_int32*data_size to 1

error_code _os_read (path_id path, void *value, u_int32 *data_size); //get current state

set u_int32*data_size to 1

(7) The Manufacturer must provide the following features to support the TOD operation and synchronization.

(a) Leap Year and Daylight Savings Time (DST) Adjustments - The OS-9 System clock / calendar must automatically be adjusted to account for DST and leap years.

(b) Setting Hardware Clock from OS-9 System Clock – Provide a device driver compatible with the OS-9 SCFMAN to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name must be “ClockUpdate.” Opening the descriptor will cause the driver to synchronize the clock to a minimum of 10 milliseconds resolution. The driver must compensate for any time elapsed during the process of updating the hardware clock.

(c) Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar must automatically be updated from the hardware TOD clock. The clocks must be synchronized to a minimum of 10 milliseconds resolution.

(8) The FLASH drive must be protected from corruption. It must be protected using the Write Protect (WP) bit of the Base Register. This bit must be set except when explicitly writing to flash. When writing to the FLASH drive the current sector of FLASH being written must first be backed up in SRAM. The backup sector copy must be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver must detect the presence of the valid backup sector copy in SRAM and read sector data from the valid backup sector copy. A user write operation must restore the valid backup sector copy first. Execution of the program module, “FLRESTORE,” in the Boot Image must also restore the valid backup sector copy to FLASH drive after a specified delay. “FLRESTORE” must accept a delay parameter in seconds ranging

from 0 to 600 seconds. The default delay factor is 30 seconds. No more that 150 KB of SRAM to be dedicated to this purpose.

Warning: Power loss or other interruption while writing to the FLASH drive may cause FLASH drive file and/or disk corruption. It is therefore strongly recommended that the FLASH drive be used to hold controller applications only.

(9) MODEL 2070-1A and 2070-1B CPU modules shall include the following set of standard OS-9 networking modules in the operating system boot image, sufficient to support network configuration, startup, and ftp and telnet servers:

spip, ip0, sptcp, tcp0 spudp, udp0, spraw, raw0, spenet, enet, netdb (dns version), ipstart, ifconfig, route, ndbmod, ftpd, ftpdc, telnetd, telnetdc, pkman, pkdrvr, pk, pks, ping, dhcp.

The boot image shall include a default inetdb module with a module revision of zero. It shall contain the following entries only.

Hosts

localhost	127.0.0.1	me

Protocols

ip	0	IP
icmp	1	ICMP
igmp	2	IGMP
tcp	6	TCP
udp	17	UDP

Services

ndp	13312/tcp	ndpd
npp	13568/tcp	nppd
echo	7/tcp	
echo	7/udp	
ftp-data	20/tcp	
ftp-data	20/udp	
ftp	21/tcp	
ftp	21/udp	
telnet	23/tcp	
telnet	23/udp	
nameserver	42/tcp	
nameserver	42/udp	
tftp	69/tcp	
tftp	69/udp	

The boot image shall include a default inetdb2 module with a module revision of zero. It shall contain the following entry only:

Interfaces

enet0 binding /spqe0/enet (no address, netmask, or broadcast)

On the MODEL 2070-1B CPU module, an OS-9 SPF Ethernet hardware driver and descriptor for the 68360 (SCC1) must be provided in the operating system Boot Image. The descriptor must be named spqe0.

The following OS-9 modules to be included in the /f0/CMDS/BOOTOBJS flash disk directory to allow for standard TCP/IP network communications using Ethernet Protocol over Ethernet hardware and/or Serial Line Internet Protocol (SLIP) or Point-to-Point Protocol over serial links:

(a) Drivers and Descriptors for PPP.

(b) Drivers and Descriptors for SLIP.

(c) LAN Comm Pak modules: spenet, enet, spip, ip0, sptcp, tcp0, spudp, udp0, spraw, raw0, sproute, route0, spipcp, ipcp0, splcp, lcp0, sphdlc, hdlc0, spslip, sps10

(d) Network modules: pkman, pkdvr, pk, pks

(e) Network Trap Handler: netdb_local, netdb_dns

(f) NFS Modules: nfs, nfsnul and nfs_devices.

The following Network utilities must be included and must reside in the /f0/CMDS directory as identified in this specification:

arp, dhcp,ftp, ftpd, ftpdc, idbdump, idbgen, rpcdbgen, ifconfig, inetd, ipstart, ndbmod, netstat, ping, route, routed, telnet, telnetdc, hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap, pppd, chat, pppauth, nfsd, mountd, and showmount.

Multi-user functionality:

The boot image init module must be configured with a “default directory name” as /f0wp. This will allow login and tsmon to provide the user with login prompt from the terminal port or from the network via a telnet session.
The following OS-9 modules to be included in the operating system boot image for the implementation of multi-user mode.

login, tsmon

Network Configuration at boot up:
The modules inetdb, inetdb2 and rpcdb must be generated by the make utility via the use of a makefile and the network configuration

files residing the /f0/ETC directory. The generated inetdb, inetdb2 and rpcdb modules to be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. Configure the modules with the network default values as defined in Section 10.B.6. (Data Key) via the interfaces.conf shell script. Provide a Utility Program named netcfg that reads the CPU Datakey for an IP Address, Subnet Mask and Default Gateway. If the Datakey is present and valid, netcfg will set the IP Address, Subnet Mask and Default Gateway of the Model 2070 Controller when executed by a user at the command line. The netcfg utility will create a new inetdb, inetdb2 and rpcdb database module based on the Datakey network parameters. The new inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The netcfg must also allow the user to read, write and display network parameters to and from the Datakey via the command line prompt. If the Datakey is not present or invalid, netcfg must display an error and exit without altering the network configuration. The netcfg utility must reside in /f0/CMDS.

Standard Microware File System Configuration:
A user name “super” with password as “user” must be defined in the password file.

The PPP and SLIP descriptors must have baud rates and ports set as follows and be stored in the /f0/CMDS/BOOTOBJS directory,

hdlc0 and spsl0 configured to use /sp1 and 38400 bps
hdlc1 and spsl1 configured to use /sp2 and 115200 bps
hdlc2 and spsl2 configured to use /sp3 and 115200 bps
hdlc3 and spsl3 configured to use /sp4 and 38400 bps

Provide a set of example configuration files consistent with the above networking modules in the /f0/ETC directory. This directory must contain the following text files.

hosts, hosts.equiv, networks, protocols, services, inetd.conf, resolv.conf, hosts.conf, rpc, interfaces.conf, routes.conf.

(10) Standard Microware File System Configuration.

(a) The 2070 must follow Standard Microware File System Configuration. A /f0/CMDS, /f0/CMDS/BOOTOBJS, /f0/ETC and /f0/SYS directories implemented. Execute permission must be included in the attributes of files in the /f0/CMDS directory. Sysgo will set its execution directory to /f0wp/CMDS prior to spawning opexec or other processes. The /f0/CMDS/BOOTOBJS must contain the modules as identified above and other customizable descriptors and modules. The

/f0/SYS must also contain the following four standard OS-9 network configuration shell script files: startspf, startnfs, loadspf and loadnfs.

(b) The /f0/SYS must contain a "password" file. The password file will follow Microware's password file format for the addition and configuration of multiuser functionality and password protection. A user name “super” with password as “user” must be defined in the password file.

(c) The utilities tar, make, vi, fixmod and mshell must be included in the /f0/CMDS directory.

c. Application Kernel.

(1) The provided software must boot OS-9 from SYSRESET. The entire program must be resident in FLASH Memory. Configure the serial port descriptors with the following defaults:

SP1 & 2	1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo
SP 3S	614.4 Kbps
SP4	9.6 Kbps, 8-bit word, 1 stop, no parity, no pause, x on and x off BOTH OFF
SP 5S	614.4 Kbps
SP 6	38.4 Kbps, 8-bit word, 1 stop and no parity

(2) Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC must be completed in less than 4 seconds. This startup time will be measured from the release of SYSRESET to the turn on of the CPU LED using a user level program named ONLED. The ONLED program must be the last module loaded into RAM and executed using opexec or a startup file.

(3) Initialization. Configure the boot image init module with the default directory name as /f0wp and sysgo as the first executable module.

Sysgo must operate as follows:

(a) Sysgo must set the execution directory to /f0wp/CMDS

(b) Sysgo must check if the backspace key (0x08) is being received on /sp4 (c50s). If received, Sysgo must:

- Fork a shell on /sp4 using the current directory.
- Remain an active process and monitor the shell for termination. If the shell does terminate, Sysgo must fork

another shell on /sp4. Unless Sysgo dies, a shell will always be provided on /sp4.

(c) If the backspace key was not received, Sysgo must check for the presence of a Datakey. If present and valid, Sysgo will check the Startup Override byte in the Datakey header.

If Startup Override is 0x01, Sysgo must:

- Fork a shell that executes a shell script stored on the Datakey in the following format. Immediately following the key header must be a 2-byte value indicating the length of the script. The script must immediately follow the length value, and be stored as ASCII text.
- If there is any error reading or starting the script or if the shell terminates with an error, Sysgo must display an error message on /sp4 and fork another shell as described in step b. If there are no errors executing the script, Sysgo must exit without forking another shell.

If Startup Override is 0x02, Sysgo must:

- Fork an executable module stored on the Datakey immediately following the header.
- If there is any error loading or forking the module, Sysgo must display an error message on /sp4 and fork a shell as described in step b. If there are no errors forking the module, Sysgo must then exit without forking a shell.

(d) If the backspace key was not received and Startup Override was not performed:

- Sysgo must fork the module named /f0wp/OPEXEC if present at /f0wp.
- If there is any error loading or forking OPEXEC, Sysgo must display an error message on /sp4 and fork a shell as described in step b. If there are no errors forking OPEXEC, Sysgo must then exit without forking a shell.

(e) If the backspace key was not received, Startup Override was not performed, and there is no OPEXEC file:

- Sysgo must fork a shell that executes a shell script named /f0wp/startup if present at /f0wp.
- If there is any error reading or starting the script or if the shell terminates with an error, Sysgo must display an error message on /sp4 and fork another shell as described in step b. If there are no errors executing the script, Sysgo must exit without forking another shell.

(f) If the backspace key was not received, Startup Override was not performed, and there is no OPEXEC and no startup file:

- Sysgo must fork a shell as described in step b.

(4) A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. ACFAIL/POWER DOWN transitions must generate an interrupt. The interrupt updates an OS-9 event named "ACFAIL". The "ACFAIL" event sets a value 1 indicating an ACFAIL condition occurred for the DOWN transition and set 0 indicating non-ACFAIL condition for the HIGH transition. The IRQ7 and auto-vector 31(7) must not be used to update the "ACFAIL" event.

In addition, the ACFAIL condition must generate the OS-9 auto-vector 30(6) interrupt service. Each interrupt service installed must exit with the "Carry Bit" set allow OS9 to propagate the ACFAIL interrupt. The Manufacturer must supply an interrupt handler at priority 255 that acknowledges and clears the interrupt.

Reserve Priority 1 for the OS-9 system.

(5) A Long Out is defined as ACFAIL transition to LOW follow by a SYSRESET going LOW. The SYSRESET going HIGH must be followed by an operating system reboot.

d. Error Handler.

(1) A Manufacturer may include an error handling routine to save troubleshooting data regarding initialization, power-up test abnormalities and other error conditions. If used, the error report must be stored in the file /r0/ErrorReport and not exceed 11 kilobytes in size.

e. Diagnostic Acceptance Test (DAT).

(1) A DAT Program must be provided resident in the 2070 Unit as the application program.

f. Re-Flash Utility. Provide a Utility Program that would allow the user to upgrade (re-flash) the Boot Image. This utility must provide the capabilities for upgrading the Operating System and drivers when available by the manufacturer. The Utility Program must provide the capability for the user to dynamically upgrade the Boot Image via the command prompt. The Manufacturer must also provide a copy in CD Memory of all files originally stored in the flash drive /f0 so that they can be reloaded as needed.

g. Deliverables.

(1) The following items will be provided to the CITY OF HOUSTON on a CD disk readable by a PC compatible computer.

(a) Specific hardware memory addresses, including FLASH, SRAM, and DRAM starting addresses, must be specified and provided. Written documentation of addresses must be in PDF form and will have the file name of “Memory Map.pdf”

(b) Copy of all provided written manuals in PDF form.

(c) Copies of the vendor kernel, platform drivers and OS-9 utility executable modules

(d) RE-FLASH Utility and the procedures for its use in PDF form. The PDF documentation of the procedures must have the file name of “Reflash Utility Procedures.pdf”.

(2) Fully commented source code of Contractor developed drivers and utilities must be provided.

(3) OS-9 compliant header files must be provided with all driver modules.

C. Type 2070-2 Field I/O Module (FI/O).

1. Type 2070-2A Module. The TYPE 2070-2A MODULE consists of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle switch); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required resident software.

2. Type 2070-2B Module. The TYPE 2070-2B MODULE consists of the Serial Communication Circuitry, VDC Power Supply, and Module Connector C12S mounted on the module front plate only.

3. Field Controller Unit (FCU). The FCU includes a programmable microprocessor/controller unit together with all required clocking and support circuitry. Provide operational software necessary to meet housekeeping and functional requirements resident in socketed firmware.

4. Parallel I/O Ports.

a. The I/O Ports must provide 64 bits of input using ground-true logic. Each input must be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and be read logic "0" when either the input current is less than 100 microamperes or the input voltage exceeds 8.5 VDC. Each input must have an internal pull-up to the Isolated +12 VDC and not deliver greater than 20 milliamperes to a short circuit to ground.

b. The I/O Ports must provide 64 bits of output.

(1) Inputs must have the following characteristics:

(a) A voltage between 0 and 4 volts will be considered the Low (True/Operate) state.

(b) A voltage greater than 8 volts will be considered the High (False) state.

(c) The transition from the **Low** state to **High** state (and vice versa) occurs between 4 and 8 volts.

(2) Outputs must have the following characteristics:

(a) The Low (True/Operate) voltage will be between 0 and 3 volts.

(b) Current sinking capability in the Low state will be at least 100 milliamperes.

(c) With an external impedance of 100 kiloOhms or greater, the transition from 4 to 16 volts (and vice versa) and be accomplished within 0.1 millisecond.

(d) The High state impedance must exceed 1 Megohms to 12 volts DC.

c. Each output must latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output must latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state must be open (logic 0). It must be possible to simultaneously assert all outputs within 100 microseconds of each other. An output circuit state not changed during a new writing will not glitch when other output circuits are updated.

5. Other Module Circuit Functions.

a. A maximum capacitive load of 100 picofarads must be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals must be derived from the LINESYNC signal.

b. Provide an External WDT “Muzzle” Jumper on the board. With the jumper in and NRESET transitions HIGH (FCU active), the FCU must output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 milliseconds for 10 seconds or due to CPU Command. When the jumper is missing (open), the feature will not apply. This feature is required to operate with the Type 210 Monitor Unit only.

c. Provide a WATCHDOG Circuit. The FIELD I/O software at Power Up with a value of 100 milliseconds must enable it. Its enabled state must be machine readable and reported in the FI/O status byte. Once

enabled, the watchdog timer must not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout will result in a hardware reset.

d. One KHz Reference. Provide a synchronizable 1 kilohertz time reference. It must maintain a frequency accuracy of +/-0.01% (+/-0.1 counts per second).

e. Provide a 32-bit MILLISECOND COUNTER (MC) for “timestamping.” Each 1 KHz reference interrupt must increment the MC.

f. Provide a LOGIC Switch resident on the module board. The switch must function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. Provide an LED on the module front panel labeled “SP3 ON”. If LED light ON, SP3 is active and available at C12S.

6. Serial Communications/Logic Circuitry.

a. System Serial Port 5 (SP5) EIA-485 signal lines must enter the I/O Module and be split into two multi-drop isolated ports. Route one to the FCU and the other converted to EIA-485, then routed to Connector C12S.

b. System Serial Port 3 (SP3) EIA-485 signal lines must enter the I/O module and be isolated, converted back to EIA-485 and then routed to connector C12S.

c. LINE SYNC and POWER DOWN lines must be split and isolated, one routed to the FCU for shut down functions and the other changed to EIA-485; then routed to connector C12S for external module use.

d. CPU RESET and POWER UP (SYSRESET) lines must be isolated and “OR’d” to form NRESET. NRESET must be used to reset FCU and other module devices. NRESET must also be converted to EIA-485 then routed to connector C12S.

e. If the Type 2070 module is a –2B, routing to FCU does not apply.

f. Isolation is between internal +5 VDC / Ground #1 and +12 VDC ISO / VDC Ground #2. +12 VDC ISO is for board power and external logic.

7. Buffers. Provide a Transition Buffer capable of holding a minimum of 1024 recorded entries. The Transition Buffer must default to empty. There must be two entry types: Transition and Rollover. The inputs must be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry must be added to the Transition Buffer. The MC must be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry must be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU module upon command.

Upon confirmation of their reception, the blocks must be removed from the Transition Buffer. The entry types are depicted as follows:

Input Transition Entry

Description	msb							lsb	Byte Number
Transition Entry Identifier	S	Input Number							1
MC Timestamp NLSB	x	x	x	x	x	x	x	x	2
MC Timestamp LSB	x	x	x	x	x	x	x	x	3

Millisecond Counter Rollover Entry

Description	msb							lsb	Byte Number
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1
MC Timestamp MSB	x	x	x	x	x	x	x	x	2
MC Timestamp NMSB	x	x	x	x	x	x	x	x	3

8. I/O Functions. Each parallel Input/Output function contains all of the functions listed below of both the Input Function and Output Function.

   a. Inputs. Input scanning must begin at I0 (bit 0) and proceed to the highest numbered input, ascending from LSB to MSB. Each complete input scan must finish within 100 microseconds. Once sampled, the logic state of an input must be held until the next input scan. Each input must be sampled 1,000 times per second. The time interval between samples must be 1 millisecond (+/-100 microseconds). If configured to report, each input that has transitioned since its last sampling must be identified by input number, transition state, and timestamp (at the time the input scan began) and be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions must be entered into the Input Transition Buffer by increasing input number. The Millisecond Counter must be sampled within 10 microseconds of the completion of the input scan.

   b. Data Filtering. If configured, the inputs must be filtered by the FCU to remove signal bounce. The filtered input signals must then be monitored for changes as noted. The filtering parameters for each input must consist of Ignore Input Flag and the ON and OFF filter samples. If the Ignore Input flag is set, no input transitions will be recorded. The ON and OFF filter samples must determine the number of consecutive samples an input must be ON and OFF, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state must be ignored. The ON and OFF filter values must be in the range of 0 to 255. A filter value of 0, for either or both values, must result in no filtering for this input. The default values for input signals after reset must be as follows:

Input Signals	Default Value
Filtering	Enabled
On and off filter values must be set to	5

Transition monitoring	Disabled (Timestamps are not logged)

c. Outputs. Simultaneous assertion of all outputs must occur within 100 microseconds. Each output must be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs must only be "ON" if the FI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs must revert to the OFF condition, and the FI/O status byte must be updated to reflect the loss of communication from the CPU Module. The data and control bits in the CPU Module-FI/O frame protocol must control each output as follows:

Output Bit Translation

Case	Output Data Bit	Output Control Bit	Function
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

In Case A above, the corresponding output must be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed must be changed within 50 microseconds after the corresponding LINESYNC transition and must remain in the same state during the entire half cycle. In Case D above, the corresponding output must be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs never change state unless configured to do so.

d. Interrupts. All interrupts must be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt must be activated by the 1 kilohertz reference once per milliseconds. An MC timestamp rollover flag set by MC rollover must be cleared only on command. LINESYNC Interrupt - This interrupt must be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt must monitor the MC interrupt and set the MC error flag if there has not been an interrupt

from the 1 kilohertz source for 0.5 seconds (>/=60 consecutive LINESYNC interrupts). The LINESYNC interrupt must synchronize the 1 kilohertz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag must be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (>/=500 consecutive millisecond interrupts).

e. Communication Service Routine. A low-level communication service routine must be provided to handle reception, transmission, and EIA-485 communication faults. The communication server must automatically:

<u>For Transmission</u>

Generate the opening and closing flags
Generate the CRC value
Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU
Provide zero bit insertion

<u>For Receiving</u>

Detect the opening and closing flags
Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module
Strip out inserted zeros
Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
Generate an interrupt if an abort sequence is received

f. Communication Processing. The task must be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission must begin within 4 milliseconds of the receipt of the received message. The time from the receipt of message to the completion of the commanded task must not exceed 70 milliseconds.

g. Input Processing. This task must process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

9. Data Communications Protocols.

a. Protocols - All communication with the CPU Module must be SDLC-compatible command-response protocol, support 0 bit stuffing, and operate at a data rate of 614.4 kilobits per second. The CPU Module must always initiate the communication and should the command frame be incomplete or in error, no FI/O response will be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification.

(1) The frame type must be determined by the value of the first byte of the message. The command frames type values 112-127 and associated response frame type values 240-255 are allocated to the manufacturer diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times must be as follows:

Frame Types

Module Command	I/0 Module Response	Description	Minimum Message Time	Maximum Message Time
0-43	128-171	Reserved for NEMA TS-2		
49	177	Request Module Status	250 microseconds	275 microseconds
50	178	MILLISECOND CTR. Mgmt.	222.5 microseconds	237.5 microseconds
51	179	Configure Inputs	344.5 microseconds	6.8750 milliseconds
52	180	Poll Raw Input Data	317.5 microseconds	320 microseconds
53	181	Poll Filtered Input Data	317.5 microseconds	320 microseconds
54	182	Poll Input Transition Buffer	300 microseconds	10.25 microseconds
55	183	Command Outputs	405 microseconds	410 microseconds
56	184	Reserved	340 microseconds	10.25 milliseconds
57	185	Reserved	340 microseconds	6.875 milliseconds
58	186	Configure Watchdog	222.5 microseconds	222.5 microseconds
59	187	Controller Identification	222.5 microseconds	222.5 microseconds
60	188	I/O Module Identification	222.5 microseconds	222.5 microseconds
61-62	189-190	Reserved (note below)	---	---
63	191	Poll variable length raw input	317.5 microseconds	320 microseconds
64	192	Variable length command outputs	405 microseconds	410 microseconds
65	193	Reserved (note below)	---	---
67	195	Reserved (note below)	---	---

(2) Messages 61 / 189, 62 / 190, 65 / 193, and 67 / 195 are reserved for ITS Cabinet Frame Types. Message 63 / Message 191 must be the same as Message 52 / 180 except Byte 2 of Message 180 response must denote the following number of input data bytes.

Message 64 / 192 must be the same as Message 55 / 183 except Byte 2 of the Message 55 Command must denote the number of output data bytes, plus the following output control bytes.

b. Request Module Status. The Command must be used to request FI/O status information response. Command/response frames are as follows:

Request Module Status Command

Description	msb							lsb	Byte Number
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	msb							lsb	Byte Number
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
MC Timestamp MSB	MC Timestamp MSB								Byte 5
MC Timestamp NMSB	MC Timestamp NMSB								Byte 6
MC Timestamp NLSB	MC Timestamp NLSB								Byte 7
MC Timestamp LSB	MC Timestamp LSB								Byte 8

(1) The response status bits are defined as follows:

P Indicates FI/O hardware reset
E Indicates a communications loss of greater than 2 seconds
K Indicates the Datakey has failed or is not present
R Indicates that the EIA-485 receive error count byte has rolled over
T Indicates that the EIA-485 transmit error count byte has rolled over
M Indicates an error with the MC interrupt
L Indicates an error in the LINESYNC
W Indicates that the FI/O has been reset by the Watchdog

(2) The FI/O status byte must be updated (set to '1') to reflect the faults noted in clause 12. Data Communications Protocols – a.(1). Each status bit must only be reset (set to '0') when the corresponding bit of the Request Module Status Command is a '1'. The Request Module Status Response must report the current status (subsequent to reset and sampling).

(3) The FI/O must count the number of errored frames the FI/O Communications Processor reports. Separate counts must be maintained for transmit and received frames. When an individual count rolls over (255-0), the corresponding roll-over flag must be set.

(4) FI/O modules with Datakey: On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O must test the presence of the Key. If absent, Status Bit “K” must be set to '1' and no interrogation take place. If an error occurs during the interrogation, Status Bit “K” must be set to '1'. FI/O modules without Datakey: Status Bit "K" must always be set to '1'

(5) The MC timestamp value must be sampled just prior to the Request Module Status Response.

c. MC Management. MC MANAGEMENT frame must be used to set the value of the MC. The 'S' bit must return status '0' on completion. The 32-bit value must be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

Millisecond Counter Management Command

Description	msb							lsb	Byte Number
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 2
New MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3
New MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 4
New MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 5

Millisecond Counter Management Response

Description	msb							lsb	Byte Number
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

d. Configure Inputs. The Configure Inputs command frame must be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	msb							lsb	Byte Number
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	n	n	n	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4

Description	msb lsb	Byte Number
Item # - Byte 3	Trailing edge filter (r)	Byte 3(I-1)+5

Configure Inputs Response

Description	msb							lsb	Byte Number
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Block field definitions must be as follows:

E Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input

e A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)

r A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)

S return status S = '0' on completion or '1' on input error out of range

e. Poll Raw Input Data. The Poll Raw Input Data frame must be used to poll the FI/O for the current unfiltered status of all inputs. The response frame must contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	msb							lsb	Byte Number
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Poll Raw Input Data Response (2070-2A)

Description	msb							lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x	Bytes 3 to 9
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 10
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Raw Input Data Response (2070-8)

Description	msb							lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

f. Poll Filtered Input Data. The Poll Filtered Input Data frame must be used to poll the FI/O for the current filtered status of all inputs. The response frame must contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs. Raw input data must be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	msb							lsb	Byte Number
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1

Poll Filter Input Data Response (2070-2A)

Description	msb							lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x	Bytes 3 to 9
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 10
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Filter Input Data Response (2070-8)

Description	msb							lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

g. Poll Input Transition Buffer. The Poll Input Transition Buffer frame must poll the FI/O for the contents of the input transition buffer. The response frame must include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	msb							lsb	Byte Number
(Type Number = 54)	0	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2

Poll Input Transition Buffer Response

Description	msb							lsb	Byte Number
(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2
Number of Entries	x	x	x	x	x	x	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+5
Item # MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(I-1)+7
MC Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+8
MC Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+9
MC Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+10
MC Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+11

(1) Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. The FI/O must set the 'F' bit to '1' when attempting to record a transition and the Transition Buffer is full. While the Transition Buffer is full, all subsequent entries must be discarded. Bit definitions are as follows:

S Indicates the state of the input after the transition
C Indicates the 255 transition entries limit has been exceeded
F Indicates the transition buffer limit has been exceeded
G Indicates the requested block number is out of monotonic increment sequence
E Same block number requested, E is set in response

(2) The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it must compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer must be re-sent to the CPU Module and the 'E' flag set in the status

response frame. If it is not equal to the previous Block Number, the old buffer must be purged and the next block of data sent. If the block number is not incremented by one, the status G bit must be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block must be the same as that received in the command block. Counter rollover must be considered as a normal increment.

(3) The Timestamp must equal the MC value at the time the Poll Input Transition Buffer Response is generated.

h. Set Outputs. The Set Outputs frame must be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame must be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame must be set. Loss of LINESYNC reference must also be indicated in system status information. The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command

Description	ms b							lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O103 Data	x	x	x	x	x	x	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	Byte 15
Outputs O8 to O103 Control	x	x	x	x	x	x	x	x	Bytes 16 to 27

Set Outputs Response

Description	msb							lsb	Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

i. Configure Watchdog. The Configure Watchdog frames must be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	msb	lsb	Byte Number

Description	msb							lsb	Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	x	x	x	x	x	Byte 2

Configure Watchdog Response

Description	msb							lsb	Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

(1) The timeout value must be in the range between 10 to 100 milliseconds. If the value is lower than 10, 10 must be assumed. If the value is greater than 100, 100 must be assumed.

(2) On receipt of this frame, the watchdog timeout value must be changed to the value in the message and the “Y” bit set. The response frame bit (Y) must indicate a '1' if the watchdog has been previously set and a '0' if not.

j. Controller Identification. This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey See previous sections on Request Module Status for FI/O Status Bit ‘K’ definition. If “K” bit set, only the first two bytes must be returned. The Command and Response frames are as follows:

Controller Identification Command

Description	msb							lsb	Byte Number
(Type Number= 59)	0	0	1	1	1	0	1	1	Byte 1

Controller Identification Response

Description	msb							lsb	Byte Number
(Type Number = 187)	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey	x	x	x	x	x	x	x	x	Bytes 3 to 130

k. Module Identification. The I/O Module Identification Command frame must be used to request the FI/O Identification value. A response of "1" must be returned by 2070-2A, "2" by 2070-8, "3" is reserved for NEMA TS 2 Type 1 FI/O and "32 to 40" are reserved for ITS Cabinets. The command and response frames are shown as follows:

I/O Module Identification Command

Description	msb							lsb	Byte Number
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

I/O Module Identification Response

Description	msb							lsb	Byte Number
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1
FI/O I D byte	x	x	x	x	x	x	x	x	Byte 2

D. Type 2070-3 Front Panel Assembly.

1. General. The Type 2070-3 Front Panel Assembly (FPA) must be delivered with one of the three options as defined in this clause. All options must consist of a panel with Latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connector(s), CPU active LED indicator, and FP Harness Interface. The options must include the additional features, as follows:

Option 3A	FPA controller, two keyboards, AUX switch, alarm bell and Display A
Option 3B	FPA controller, two keyboards, AUX switch, alarm bell and Display B - required for NEMA compliance (TS-1 & TS-2 type1) 8 x 40 display with 2 keypads
Option 3C	System Serial Port 6 Lines, isolated and vectored to Connector C60S.

2. Keyboards. Provide two KEYBOARDS , one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Engrave or emboss each key with its function character. Each key must have an actuation force between 50 and 100 grams and provide a positive tactile indication of contact closure. Key contacts must be hermetically sealed, have a design life of over one million operations, be rated for the current and voltage levels used, and stabilize within 5 milliseconds following contact closure.

3. CPU Active Indicator. The cathode of the CPU ACTIVE LED INDICATOR must be electrically connected to the CPU Activity LED signal and be pulled up to +5 VDC.

4. Display. The DISPLAY must consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A must have 4 lines of 40 characters each with a minimum character dimensions of 0.20 inches wide by 0.41 inches high and an electro -luminescent (EL) backlight. Display B must have 8 lines of 40 characters each with minimum dimensions of 0.10 inches wide by 0.17 high and either LED or EL backlight.

   a. Each character must be composed of a 5 x 7 dot matrix with an underline row or a 5 x 8 dot matrix. The viewing angle of the LCD must be optimized for direct (90 degrees) viewing, +/-35 degrees vertical, +/-45 degrees horizontal. The LCD must have variable contrast with a

minimum ratio of 4:1. The LCD must be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

b. The backlight must be turned on and off by the Controller Circuitry. The backlight and associated circuitry must consume no power when in off state. A potentiometer must control the LCD contrast with clockwise rotation increasing contrast. The contrast must depend on the angular position of the potentiometer, which must provide the entire contrast range of the LCD.

c. Cursor display must be turned ON and OFF by command. When ON, the cursor must be displayed at the current cursor position. When OFF, no cursor is to be displayed. All other cursor functions (positioning, etc.) must remain in effect.

5. FPA Controller. The FPA CONTROLLER must function as the Front Panel Device controller interfacing with the CPU Module.

a. Provide a FPA RESET Switch on the Assembly PCB. The momentary CONTROL switch must be logic OR'd with the CPU RESET Line, producing a FPA RESET Output. Upon FPA RESET being active or receipt of a valid Soft Reset display command, the following must occur:

(1) Auto-repeat, blinking, auto-wrap, and auto-scroll must be set to OFF.

(2) Each special character must be set to ASCII SPC (space).

(3) The tab stops must be set to columns 9, 17, 25, and 33.

(4) The backlight timeout value must be set to 6 (60 seconds).

(5) The backlight must be extinguished.

(6) The display must be cleared (all ASCII SPC).

(7) The FPA module must transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware RESET BUTTON IS PUSHED. The string is “ESC [PU”, hex value “1B 5B 50 55”.

b. When a keypress is detected, the appropriate key code must be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code is to be sent. If a key is depressed while another key is depressed, no additional code is to be sent.

c. Auto-repeat must be turned ON and OFF by command. When ON, the key code must be repeated at a rate of 5 times per second starting

when the key has been depressed continuously for 0.5 second, and must terminate when the key is released or another key is pressed.

d. When the AUX Switch is toggled, the appropriate AUX Switch code must be transmitted to the CPU.

e. The controller circuitry must be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters must be ignored. User-composed characters must be represented in the communication protocol on Page 9-7-12. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit must represent the bottom pixel. A logic ‘1’ must turn the pixel ON. There must be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's must be ignored. P1 and all Pn's must be in ASCII coded decimal characters without leading zero.

f. Character overwrite mode must be the only display mode supported. A displayable character received must always overwrite the current cursor position on the Display. The cursor must automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position must be determined based on the current settings of the auto-wrap mode.

g. Auto-wrap must be turned ON & OFF by command. When ON, a new line operation must be performed after writing to position 40. When OFF, upon reaching position 40, input characters must continue to overwrite position 40.

h. Cursor positioning must be non-destructive. Cursor movement must not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

i. Blinking characters must be supported, and be turned ON and OFF by command. When ON, all subsequently received displayable characters must blink at the rate of 1 Hertz with a 60% ON / 40% OFF duty cycle. It must be possible to display both blinking and non-blinking characters simultaneously.

j. Tab stops must be configurable at all columns. A tab stop must be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) must be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor must move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor must not move.

k. Auto-scroll must be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line must result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line must result in the top line clearing, and the cursor being positioned on the top line.

l. The display must have a buffer. The screen must be refreshed from the buffer at a rate of no less than 20 times per second.

m. The Display back light must illuminate when any key is pressed and illuminate or extinguish by command. The backlight must extinguish when no key is pressed for a specified time. This time must be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 must correspond to a timeout interval of 10 seconds. A value of 0 must indicate no timeout.

n. The Command Codes must use the following conventions:

(1) Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.
P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)
Px: Display column number (1-40), using one ASCII character per digit without leading zero.
Py: Display line (1-4) one ASCII character
...: Continue the list in the same fashion

Values of 'h' (0x68) and 'l' (0x6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

(2) ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

(3) Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 0x00 to 0x7F (7 bits).

o. The Controller Circuit must communicate via a SP6 asynchronous serial interface. The interface must be configured for 38.4 kilobits per second, 8 data bits, 1 stop bit, and no parity.

p. C50 ENABLE function when grounded by pins 1 and 5, must be brought to Connectors A1, pin B21 for the purpose of disabling the module channel 2, (SP4).

6. Electronic Bell. The Front Panel must include an electronic bell to signal receipt of (0x07). The bell must sound at 2,000 Hertz, with a minimum output rating of 85 dB upon receipt of (0x07). Receipt of all other characters and ESC codes must continue during the time the bell sounds.

E. Type 2070-4 Power Supply Module.

1. General. The Type 2070-4A Power Supply Module must be independent, self contained Module, vented, and cooled by convection only. The Module must slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices.

   a. The Type 2070-4B Module must meet the same requirements as the 2070-4A, except for 3.5 amperes of +5 VDC.

2. Module Front. An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection must be provided on the Module Front. The LED DC POWER Indicators must indicate all required DC voltages meet the following conditions: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.

3. Input Protection. Provide two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 micro Henries inductance (one on the AC+ Line & on the AC- Line). Provide three 20 Joule surge arrestors between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor must be placed between AC+ & AC- (between the resistor & arrestors).

4. +5VDC Standby Power. Provide +5 VDC STANDBY POWER to hold up specified circuitry during the power down period. It must consist of the monitor circuitry, hold up capacitors, and charging circuitry. Provide a charging circuit that under normal operation, fully charges and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements must be a minimum constant drain of 600 microamperes at a range of +5 VDC to +2 VDC for over 600 minutes.

5. Monitor Circuitry. Provide MONITOR CIRCUITRY to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

   a. The ACFAIL/POWER DOWN Output Lines must go LOW (ground true) immediately upon Power Failure. The Lines must transition to HIGH at Power Restoration. The Lines must be driven separately. The SYSRESET/POWERUP Output Lines must transition to LOW 525 +/-25 milliseconds after ACFAIL/POWER DOWN transition to LOW. The Lines must transition to HIGH 225 +/-25 milliseconds after Power

Restoration and the supply is fully recovered. The Lines must be driven separately.

b. The monitor circuitry must switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

c. The 60 Hz Square Wave LINESYNC signal must be generated by a crystal oscillator, which must be synchronized to the 60-Hertz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal must be +5 VDC amplitude, 8.333 milliseconds half-cycle pulse duration, and 50 +/-1% duty cycle. The output must have drive sink capability of 16 milliamperes. A 2 K-Ohm pull-up resistor must be connected between the output and +5 VDC. The monitor circuit must compensate for missing pulses and line noise during normal operation.

d. The LINESYNC must continue until SYSRESET transitions LOW and begin when SYSRESET transitions HIGH.

6. Power Supply Requirements.

Voltage	Tolerances	I Minimum	I Maximum
+5 VDC	+4.875 to +5.125 VDC	1.0 ampere	10.0 ampere- MODULE 2070-4A 3.5 ampere– MODULE 2070-4B
+12 VDC Serial	+11. 4 to +12. 6 VDC	0.1 ampere	0.5 ampere
-12 VDC Serial	-11. 4 to –12. 6 VDC	0.1 ampere	0.5 ampere
+12 VDC	+11. 4 to +12. 6 VDC	0.1 AMP	1.0 AMP

a. Line/Load Regulation. Line / Load Regulation must meet the table tolerance values for voltage range of 90 to 135 VAC, the maximum and minimum loads called out in the table and including ripple noise.

b. Efficiency. 70% minimum.

c. Ripple and Noise. Less than 0.2% RMS, 1% peak to peak or 50 millivolts, whichever is greater.

d. Voltage Overshoot. No greater than 5%, all outputs.

e. Overvoltage Protection. 130% V out for all outputs.

f. Circuit Protection. Automatic recovery upon removal of fault.

g. Inrush Current. Cold Start Inrush must be less than 25 amperes at 115VAC.

h. Transient Response. Output voltage back to within 1% in less than 500 microseconds on a 50% Load change. Peak transient not to exceed 5%.

i. Holdup Time. The power supply must supply 30 watts minimum for 550 milliseconds after ACFAIL going LOW. The supply must be capable of holding up the Unit for two 500 milliseconds Power Loss periods occurring in a 1.5-second period.

j. Remote Sense. +5 VDC compensates 250 millivolts total line drop. Open sense load protection required.

F. Unit Chassis and Type 2070-5 VME Cage Assembly.

1. General.

a. The Chassis consists of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s).

b. All external screws must be countersunk and be Phillips flat head stainless steel type.

c. The housing must be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide.

d. The Chassis must be cooled by convection only. The top and bottom pieces of the housing must be slotted for vertical ventilation.

2. Serial Motherboard. Serial Motherboard must function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB must be multi-layered, with one layer plane assigned to DC Ground.

a. A wiring harness PS2 must be provided between the Type 2070-4 Power Supply and the Motherboard PCB (provide strain relief). Test points must be provided on the FPA side of the Motherboard for PS2 lines.

b. A wiring harness FP must be provided, linking the Motherboard with the FPA.

3. Type 2070-5 VME Cage Assembly. Type 2070-5 VME Cage Assembly must consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. The VME Cage must conform to VME Standard IEEE P1014/D12 for 3U Cage. All slot/connectors must be A24:D16 Interface.

4. Type 2070-1A CPU Main Controller Board. The Type 2070 – 1A CPU Main Controller Board must either be affixed to the Transition Board via at least

four stand-off devices or mounted in a one slot VME board assembly (removable). A PS1L Harness must be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector. A 100-Ohm resistor per line must terminate the VME bus lines.

G. Details.

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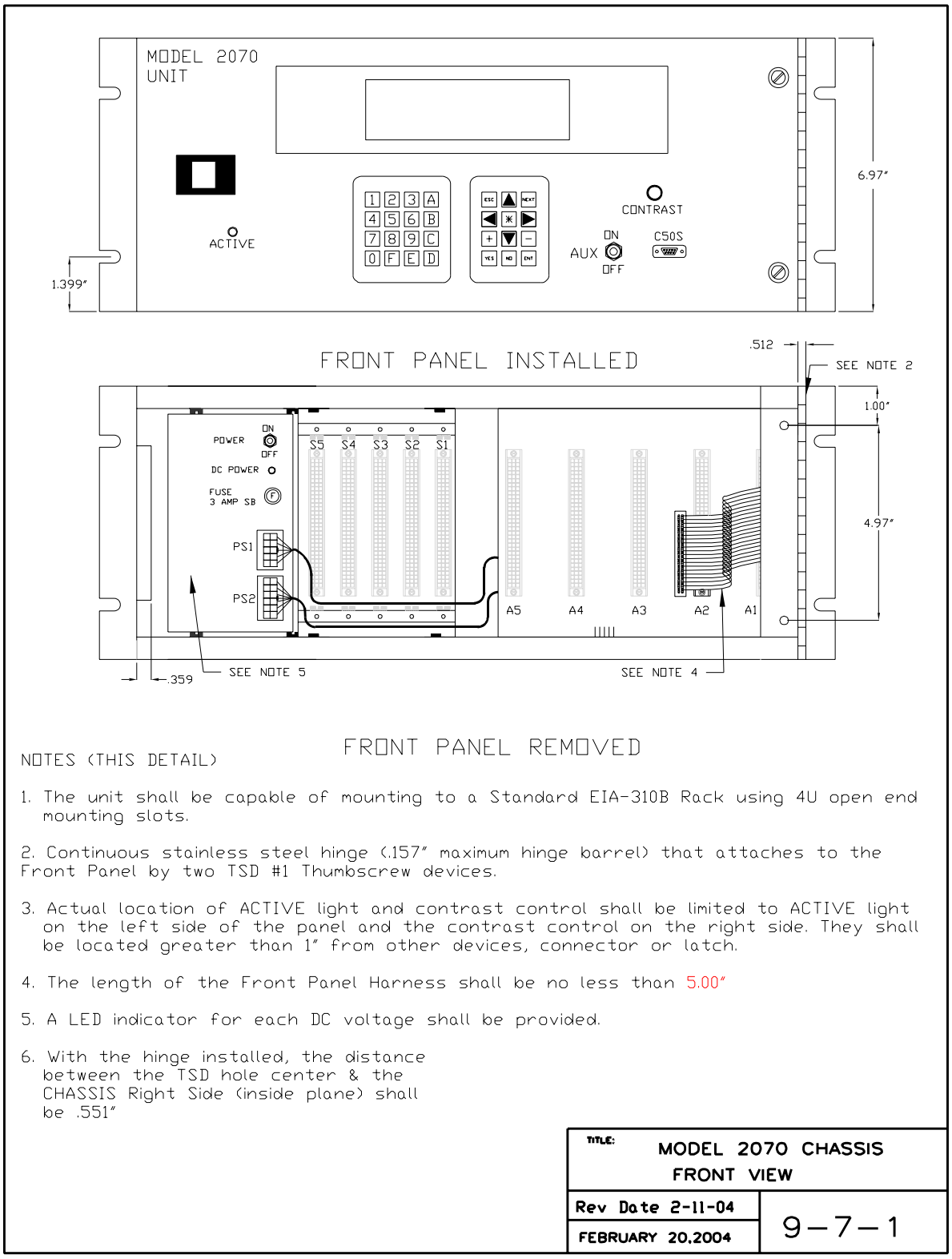


NOTES (THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.

2. Continuous stainless steel hinge (.157" maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.

3. Actual location of ACTIVE light and contrast control shall be limited to ACTIVE light on the left side of the panel and the contrast control on the right side. They shall be located greater than 1" from other devices, connector or latch.

4. The length of the Front Panel Harness shall be no less than 5.00"

5. A LED indicator for each DC voltage shall be provided.

6. With the hinge installed, the distance between the TSD hole center & the CHASSIS Right Side (inside plane) shall be .551"

TITLE: MODEL 2070 CHASSIS FRONT VIEW	
Rev Date 2-11-04	9-7-1
FEBRUARY 20,2004	

Figure 3
Chassis Front View
16731-78
01/14/2008

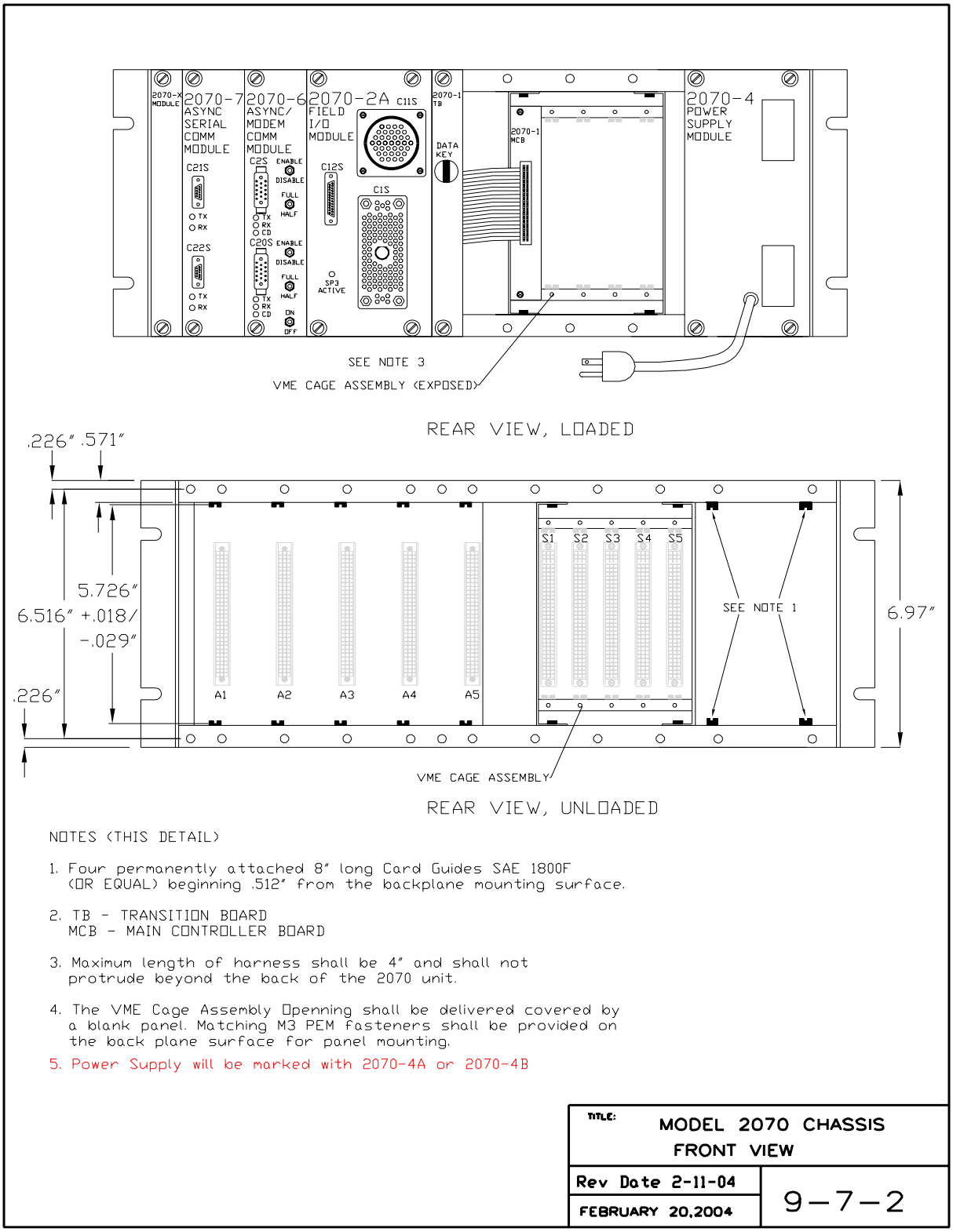
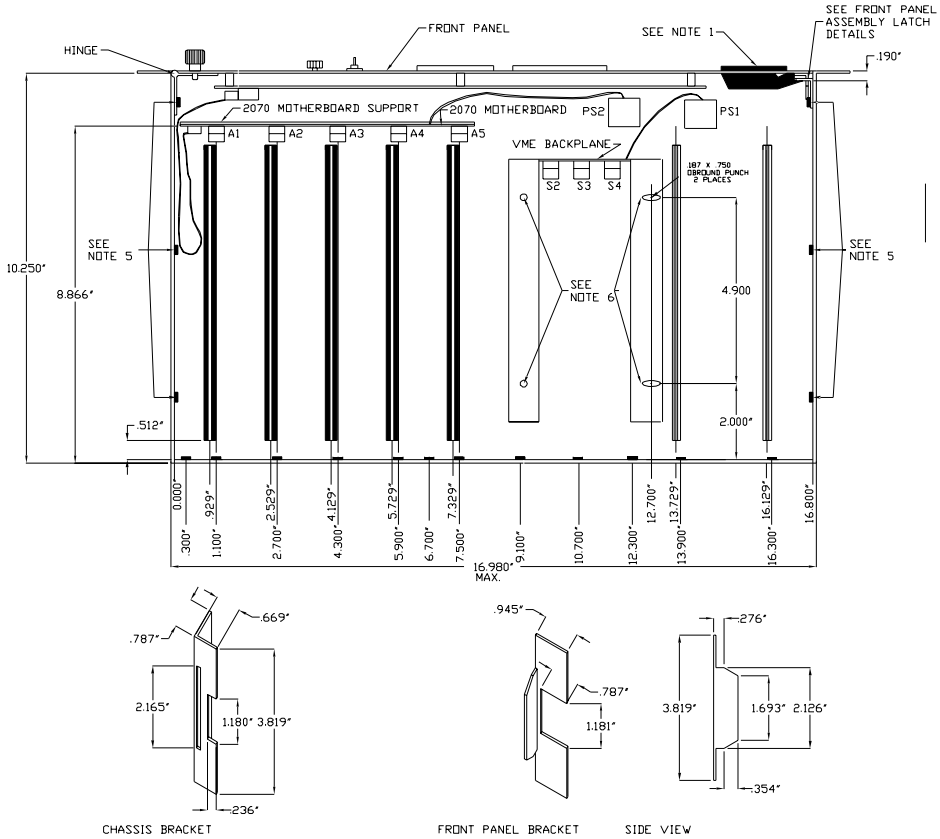


Figure 4
Chassis Rear View
16731-79
01/14/2008



NOTES (THIS DETAIL)

FRONT PANEL ASSEMBLY LATCH DETAILS

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided. The member shall vertically support the Front Panel Assembly in two other points besides the Latch.

2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin .512" from the Backplane surface.

3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.

4. All harnesses shall have a minimum slack of 1.00" when connected.

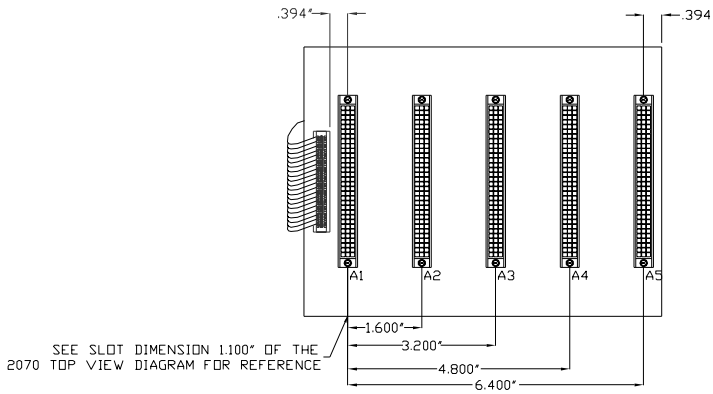
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Model 2070-8 Module. Fastener centers shall be .250" above unit baseline.

6. Eight 6-32 Phillips head counter-sunk screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.

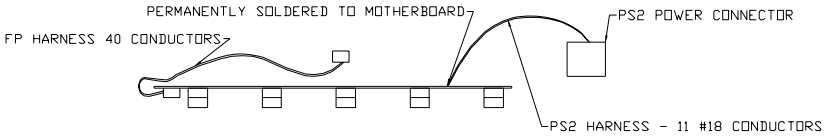
7. The 2070 chassis top & bottom sections shall be constructed with a continuous .621" folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed .709" as measured from the front surface of the front panel.

TITLE: MODEL 2070 CHASSIS TOP VIEW	
Rev Date 2-11-04	9-7-3
FEBRUARY 20,2004	

Figure 5
Chassis Top View



FRONT VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4-TXD+	2	SP4-TXD-
3	SP4-RXD+	4	SP4-RXD-
5	SP6-TXD+	6	SP6-TXD-
7	SP6-RXD+	8	SP6-RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DC GROUND #1	22	DC GROUND #1
23	+12 VDC SERIAL	24	-12 VDC SERIAL
25	DC GROUND #1	26	DC GROUND #1
27	CPU LED	28	DC GROUND #1
29	CPURESET	30	DC GROUND #1
31	DC GROUND #1	32	C50 ENABLE
33	DC GROUND #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC - ISOLATED
7	DC GROUND #2 (+12 VDC ONLY)
8	POWER DOWN
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a .125" minimum thickness pcb mounted in a vertical position.

2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).

3. The FP Harness may be located on either side of the motherboard. The FP Harness shall either be directly soldered to the motherboard or a header used.

TITLE: MODEL 2070 CHASSIS MOTHERBOARD	
Rev Date 2-11-04	9-7-4
FEBRUARY 20, 2004	

Figure 6
Chassis Motherboard

A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXCO+	SP5RXD+
6	SP3RTS-	SP3TXCO-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXCO+
20	NA	NA	SP3TXCO-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXCO+	SP3CTS+
16	SP2RTS-	SP2TXCO-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXCO+
20	SP2DCD-	SP2RXC-	SP3TXCO-
21	DCG #1	NA	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

NOTES (THIS DETAIL)

1. Functions are referenced to the CPU.
2. DC GND #1 for +5VDC and +12VDC Serial. DC GND #2 for +12VDC ISO.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back. All A Connectors are pin assigned the same.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".
   Connector A2, pins B23 shall read "A2 Installed".
   Connector A3, pins B23 shall read "A3 Installed".
   Connector A4, pins B23 shall read "NA".
   Connector A5, pins B21 shall read "A2 Installed".
   Connector A5, pins B22 shall read "DCG #1".
   Connector A5, pins B23 shall read "A3 Installed".
5. Pin A24 (DCG #1) is reserved for network protection only, ie., "Ethernet Shield".
6. Connector A2 installed, enables SP1 and SP2.
7. Connector A3 install, enbales SP5.
8. SP3 and SP6 are always enabled.
9. C50 enabled, disconnects SP4 on connector A1.

TITLE: Motherboard A Connector Pin Assignment	
Rev Date 2-11-04	9-7-5
FERBUARY 20, 2004	

Figure 7
Motherboard A Connector Pin Assignment

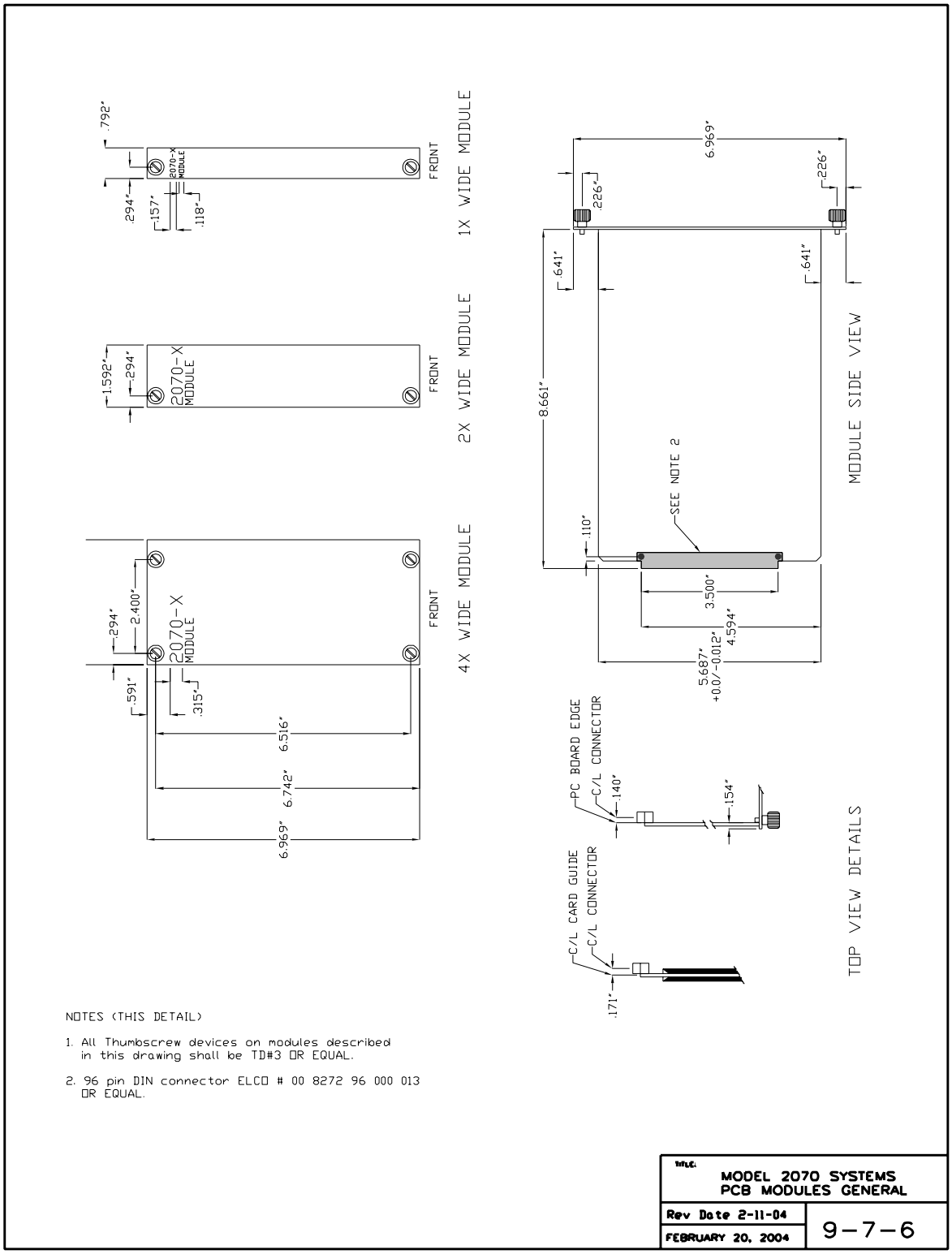
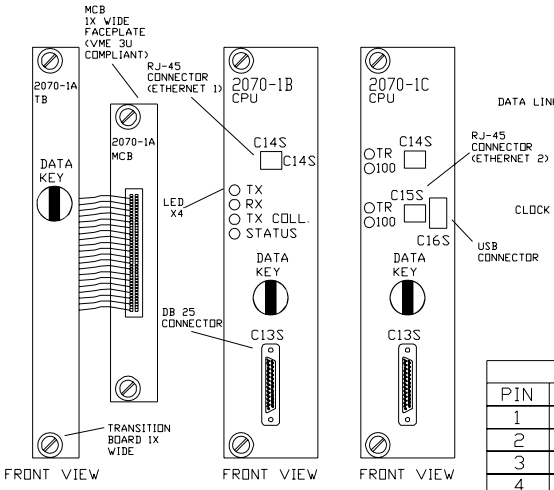


Figure 8
System PCB Modules General

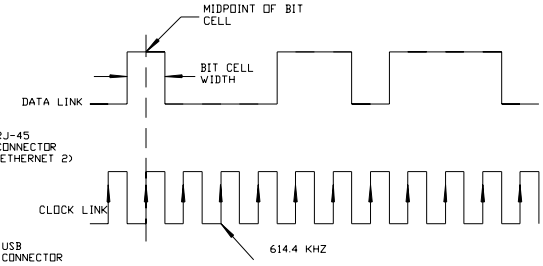
SERIAL PORT REQUIREMENTS

A2 TO A5 CONNECTOR PIN OUT			
LOGICAL PORT	68360 PORT	RATE KBITS	PROTOCOL
SP1	SEE NOTE 4	(1)	ASYNC
SP1S	SEE NOTE 4	(2)	SYNC, HDLC, SDLC
SP2	SCC2	(1)	ASYNC
SP2S	SCC2	(2)	SYNC, HDLC, SDLC
SP3	SCC4	(1)	ASYNC
SP3S	SCC4	153.6, 614.4*	SYNC, HDLC, SDLC
SP4	SMC2	(1), 9.6*	ASYNC
SP5	SCC3	(1)	ASYNC
SP5S	SCC3	153.6, 614.4*	SYNC, HDLC, SDLC
SP6	SMC1	(1), 38.4*	ASYNC
SP8**	SEE NOTE 4	9.6**	ASYNC
SP8**	SEE NOTE 4	153.6, 614.4	SYNC, HDLC. SDLC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS + **	18	SP8 RTS - **
6	SP8 CTS + **	19	SP8 CTS - **
7	SP8 DCD + **	20	SP8 DCD - **
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

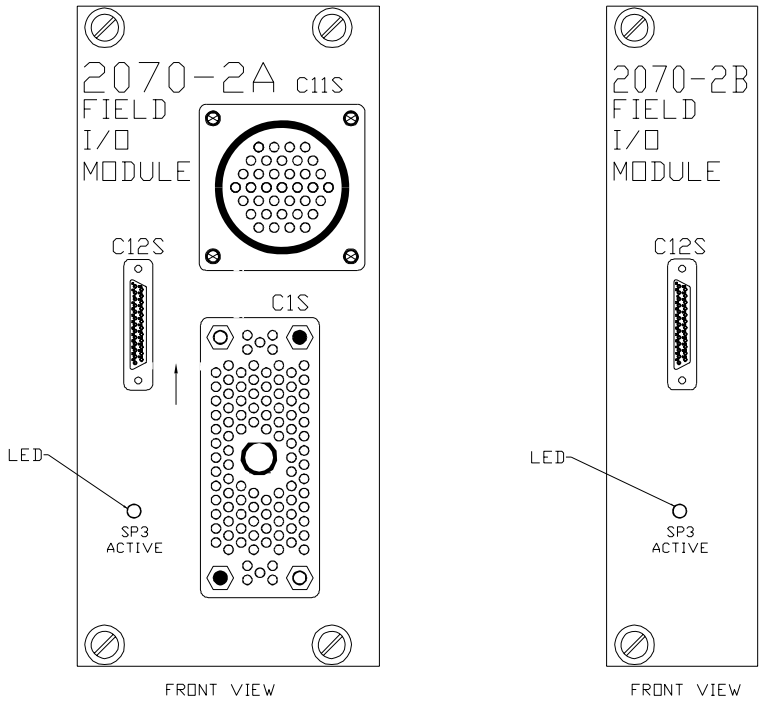
NOTES (THIS DETAIL)

1. (1) BPS Rates 1.2* 2.4, 4.8, 9.6, 19.2, 38.4
2. (2) BPS Rates 19.2*, 38.4, 57.6, 76.8, 153.6
3. * Default BPS Rate for indicated Port.
4. SP1 OF THE 2070-1A is 68360 SCC1. SP1 OF 2070-1B, -1C is Dual SCC1 with 68360 SCC1 assigned to ETHERNET. SP8 of the 2070-1B, -1C assigned to the Dual SCC.
5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.
6. ** 2070-1B, -1C only

C14S and C15S PIN ASSIGNMENT (ETHERNET)			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

TITLE: MODEL 2070-1C CPU	
Rev Date 11-4-05	9-7-7
FEBRUARY 4,2005	

Figure 9
2070-1A, 2070-1B and 2070-1C CPU Modules



FIELD I/O FACE PANELS

NOTES (THIS DETAIL)

1. 2070-2A Faceplate shall be 4X wide. 2070-2B Faceplate shall be 2X wide. (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Circles in the C1S Connector denote guide pin locations and open circles denote guide socket locations.

3. Dimension "A" shall be a minimum of .50".

4. C1S - M104 Type
   C11S - 37-Pin Circular Plastic Type
   C12S - 25-Pin DB Socket Type

5. C12S PIN 12 (+5VDC) IS DERIVED from +12 VDC Power Supply

C12S PIN ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION
1	TX5 DATA +	14	TX5 DATA -
2	RX5 DATA +	15	RX5 DATA -
3	TX5 CLOCK +	16	TX5 CLOCK -
4	RX5 CLOCK +	17	RX5 CLOCK -
5	TX3 DATA +	18	TX3 DATA -
6	RX3 DATA +	19	RX3 DATA -
7	TX3 CLOCK +	20	TX3 CLOCK -
8	RX3 CLOCK +	21	RX3 CLOCK -
9	LINE SYNC +	22	LINE SYNC -
10	NRESET +	23	NRESET -
11	POWER DOWN +	24	POWER DOWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

TITLE: MODEL 2070-2
FIELD I/O MODULES

Rev Date 2-11-04
FEBRUARY 20, 2004

9-7-8

Figure 10
Field I/O Modules

16731-85
01/14/2008

C1S PIN ASSIGNMENT

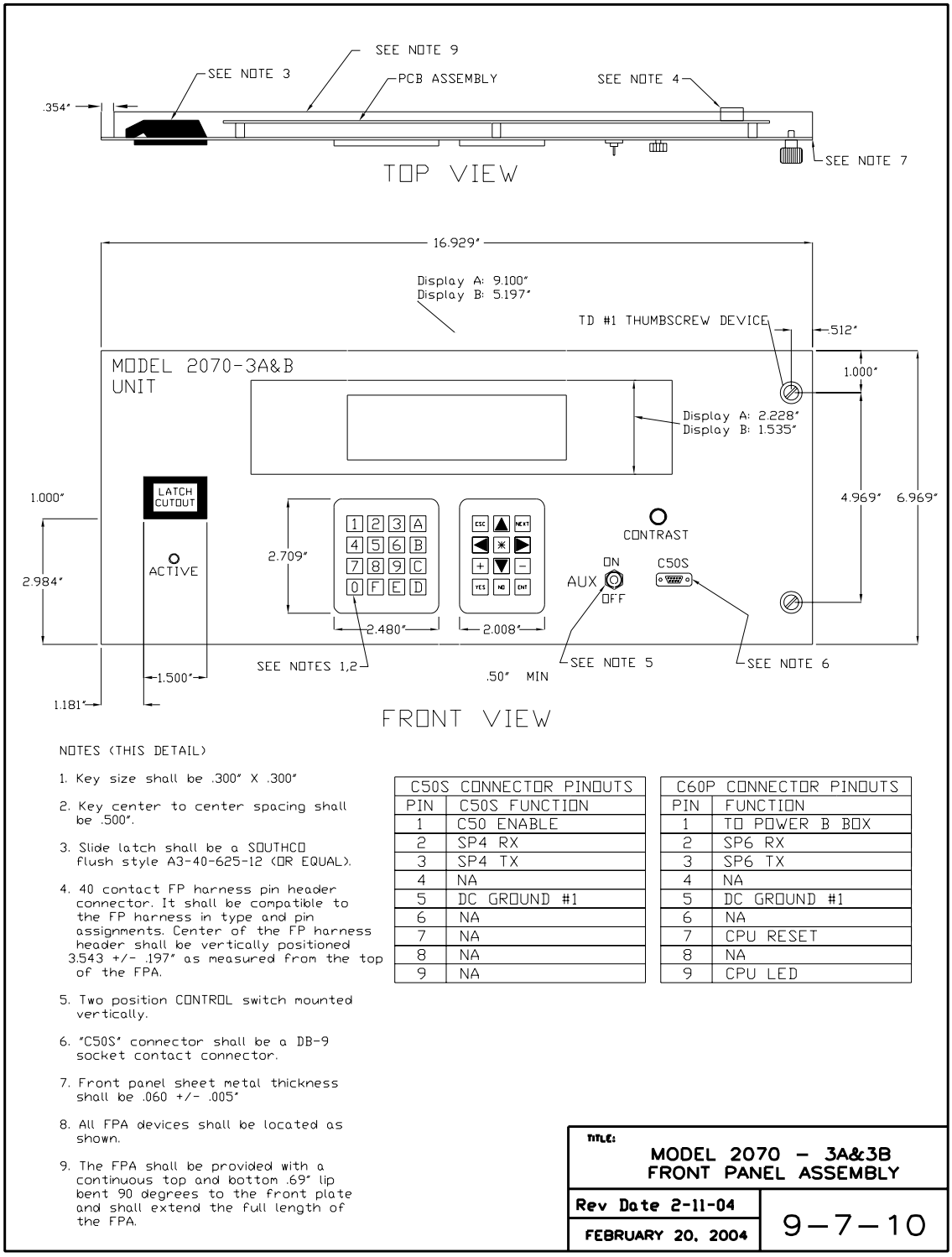
PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT
1	DC GROUND		27	O24	O4-1	53	I14	I2-7	79	I44	I6-5
2	O0	O1-1	28	O25	O4-2	54	I15	I2-8	80	I45	I6-6
3	O1	O1-2	29	O26	O4-3	55	I16	I3-1	81	I46	I6-7
4	O2	O1-3	30	O27	O4-4	56	I17	I3-2	82	I47	I6-8
5	O3	O1-4	31	O28	O4-5	57	I18	I3-3	83	O40	O6-1
6	O4	O1-5	32	O29	O4-6	58	I19	I3-4	84	O41	O6-2
7	O5	O1-6	33	O30	O4-7	59	I20	I3-5	85	O42	O6-3
8	O6	O1-7	34	O31	O4-8	60	I21	I3-6	86	O43	O6-4
9	O7	O1-8	35	O32	O5-1	61	I22	I3-7	87	O44	O6-5
10	O8	O2-1	36	O33	O5-2	62	I23	I3-8	88	O45	O6-6
11	O9	O2-2	37	O34	O5-3	63	I28	I4-5	89	O46	O6-7
12	O10	O2-3	38	O35	O5-4	64	I29	I4-6	90	O47	O6-8
13	O11	O2-4	39	I0	I1-1	65	I30	I4-7	91	O48	O7-1
14	DC GROUND		40	I1	I1-2	66	I31	I4-8	92	DC GROUND	
15	O12	O2-5	41	I2	I1-3	67	I32	I5-1	93	O49	O7-2
16	O13	O2-6	42	I3	I1-4	68	I33	I5-2	94	O50	O7-3
17	O14	O2-7	43	I4	I1-5	69	I34	I5-3	95	O51	O7-4
18	O15	O2-8	44	I5	I1-6	70	I35	I5-4	96	O52	O7-5
19	O16	O3-1	45	I6	I1-7	71	I36	I5-5	97	O53	O7-6
20	O17	O3-2	46	I7	I1-8	72	I37	I5-6	98	O54	O7-7
21	O18	O3-3	47	I8	I2-1	73	I38	I5-7	99	O55	O7-8
22	O19	O3-4	48	I9	I2-2	74	I39	I5-8	100	O36	O5-5
23	O20	O3-5	49	I10	I2-3	75	I40	I6-1	101	O37	O5-6
24	O21	O3-6	50	I11	I2-4	76	I41	I6-2	102	O38 DET RES	O5-7
25	O22	O3-7	51	I12	I2-5	77	I42	I6-3	103	O39 WDT	O5-8
26	O23	O3-8	52	I13	I2-6	78	I43	I6-4	104	DC GROUND	

C11S PIN ASSIGNMENT

PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT
1	O56	O8-1	11	I25	I4-2	21	I54	I7-7	31	DC GROUND	
2	O57	O8-2	12	I26	I4-3	22	I55	I7-8	32	NA	- - -
3	O58	O8-3	13	I27	I4-4	23	I56	I8-1	33	NA	- - -
4	O59	O8-4	14	DC GROUND		24	I57	I8-2	34	NA	- - -
5	O60	O8-5	15	I48	I7-1	25	I58	I8-3	35	NA	- - -
6	O61	O8-6	16	I49	I7-2	26	I59	I8-4	36	NA	- - -
7	O62	O8-7	17	I50	I7-3	27	I60	I8-5	37	DC GROUND	
8	O63	O8-8	18	I51	I7-4	28	I61	I8-6			
9	DC GROUND		19	I52	I7-5	29	I62	I8-7			
10	I24	I4-1	20	I53	I7-6	30	I63	I8-8			

TITLE: MODEL 2070-2A FIELD I/O MODULE C1 & C11 CONNECTORS	
Rev Date 2-11-04	9-7-9
FEBRUARY 20, 2004	

Figure 11
Field I/O Module, C1 & C11 Connectors



NOTES (THIS DETAIL)

1. Key size shall be .300" X .300"
2. Key center to center spacing shall be .500".
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. 40 contact FP harness pin header connector. It shall be compatible to the FP harness in type and pin assignments. Center of the FP harness header shall be vertically positioned 3.543 +/- .197" as measured from the top of the FPA.
5. Two position CONTROL switch mounted vertically.
6. "C50S" connector shall be a DB-9 socket contact connector.
7. Front panel sheet metal thickness shall be .060 +/- .005"
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom .69" lip bent 90 degrees to the front plate and shall extend the full length of the FPA.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

C60P CONNECTOR PINOUTS	
PIN	FUNCTION
1	TO POWER B BOX
2	SP6 RX
3	SP6 TX
4	NA
5	DC GROUND #1
6	NA
7	CPU RESET
8	NA
9	CPU LED

TITLE:
MODEL 2070 - 3A&3B
FRONT PANEL ASSEMBLY

Rev Date 2-11-04
FEBRUARY 20, 2004

9-7-10

Figure 12
Front Panel Assembly

16731-87
01/14/2008

MODEL 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

MODEL 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	OD

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY KEY CODES	
Rev Date 2-11-04	9-7-11
FEBRUARY 20, 2004	

Figure 13
Front Panel Assembly Key Codes

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn…f	1B 50 P1 5B Pn 3B…Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A & B.
Commends shall be available for option 3C (C60).

INQUIRY COMMAND-RESPONSE CODES

COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY KEY CODES	
Rev Date 2-11-04	9-7-12
FEBRUARY 20, 2004	

Figure 14
Front Panel Assembly Key Codes

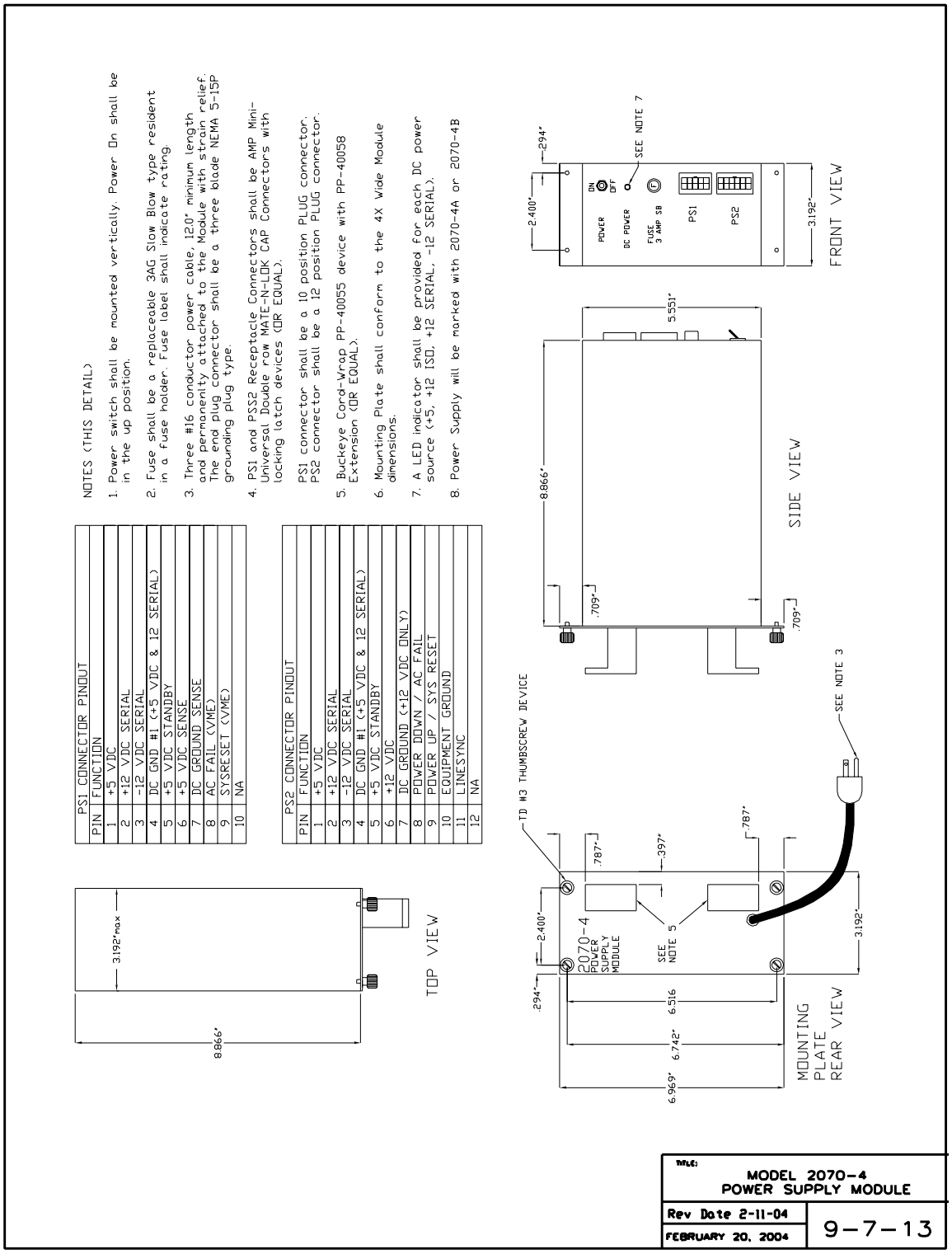
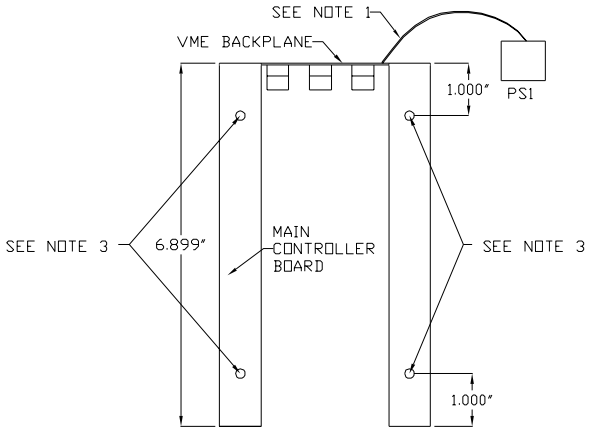


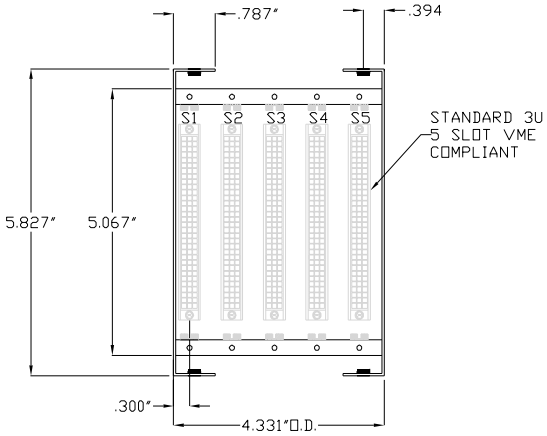
Figure 15
Power Supply Module

16731-90
01/14/2008



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA



FRONT VIEW

NOTES (THIS DETAIL)

1. PS1 Harness interfaces between the Model 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FASTON or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The plate shall cover the open area & attach to the Chassis Backplane mounting surface via screws meeting the Chapter 1 external screw requirements. The screws shall mate with the PEM nuts as specified in the Model 2070 Chassis Top View Detail.

3. G-32 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 screws on the top and bottom of the Model 2070 chassis.

TITLE: MODEL 2070-5 VME CAGE ASSEMBLY	
Rev Date 2-11-04	9-7-14
FEBRUARY 20, 2004	

Figure 16
VME Cage Assembly

2.08 TYPE 2070 PERIPHERAL EQUIPMENT

A. General Notes.

1. The 2070-6x and 2070-7x modules must provide circuitry to disable its Channel 2 and EIA-232 control lines (TX, RX, RTS, CTS, and DCD) when a ground true state is present at Connector A1, Pin B21 (C50 Enable). The disable lines must be pulled up on this module.

2. Line drivers/receivers must be socket mounted or surface mounted.

3. Isolation circuitry must be opto- or capacitive-coupled isolation technologies. Each module's circuit must be capable of reliably passing a minimum of 1.0 megabits per second.

4. The Comm modules must be "Hot" swappable without damage to circuitry or operations.

B. Type 2070-6 A & B Async/ Modem Serial Comm Modules

1. Power Requirements. A fused isolated +5 VDC with a minimum of 100 milliamperes power supply must be provided for external use.

   Option – Bourns MF – MSMD020 PTC (Positive Temperature Coefficient) Resettable Fuse, or approved equal, allowed.

2. Logic Switches. Two LOGIC switches per circuit must be provided (faceplate mounted).

   a. One logic switch must be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections must be used for both Receive and Transmit.

   b. A MODEM Enable switch must be provided such that when in the UP Position must enable MODEM and disable MODEM in the DOWN Position.

3. Circuitry. Two circuits, designated CIRCUIT #1 and CIRCUIT #2, must be provided. Both circuit functions must be identical, except for their Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and C2S Connector and CIRCUIT #2 to SP2 [or SP4] and C20S Connector). The Circuits must convert the 2070 UNIT Motherboard SP EIA-485 signals to/from board TTL level signals, isolate and drive the converted EIA-232 Signals interfacing with their associated MODEM and external connector.

   a. Modem Requirements. Each CIRCUIT must have a MODEM with the following requirements:

      (1) Data Rate: Baud modulation of 300 to 1200 for Module 2070-6A and 0 to 9600 for Module 2070-6B.

(2) Modulation: Phase coherent frequency shift keying (FSK).

(3) Data Format: Asynchronous, serial by bit.

(4) Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive):2070-6A - 1.2 KHz MARK and 2.2 KHz SPACE, +/-1% tolerance. 2070-6B - 11.2 KHz MARK and 17.6 KHz SPACE, +/-1% tolerance. The operating band must be (half power, -3 dB) between 1.0 KHz & 2.4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.

(5) Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A & 14.7 KHz for 2070-6B) continuous or switch selectable.

(6) Receiver Input Sensitivity: 0 to -40 dB.

(7) Receiver Bandpass Filter: Must meet the error rate requirement specified below and provide 20 dB/octave, minimum active attenuation for all frequencies outside the operating band.

(8) Clear-to-Send (CTS) Delay: 11 +/-3 milliseconds.

(9) Receive Line Signal Detect Time: 8 +/-2 milliseconds mark frequency.

(10) Receive Line Squelch: 6.5 (+/-1) milliseconds, 0 milliseconds (OUT).

(11) Soft Carrier Turn Off Time: 10 +/-2 milliseconds (0.9 kilohertz for 2070-6A and 7.8 kilohertz for 2070-6B). When the RTS is unasserted, the carrier must turn off or go to soft carrier frequency.

(12) Modem Recovery Time: Capable of receiving data within 22 milliseconds after completion of transmission.

(13) Error Rate: Must not exceed 1 bit in 100 kilobits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hertz band.

(14) Transmit Noise: Less than -50 dB across 600-ohms resistive load within the frequency spectrum of 300 to 3,000 Hertz at maximum output.

(15) Modem interface: EIA-232 Standards.

4. Control Switch. A CONTROL switch must be provided on the module front panel to turn ON (Up) / OFF (Down) all module power.

C. Type 2070-7A & 7B Async Serial Comm Module

1. Circuitry. Two circuits, designated CIRCUIT #1 and CIRCUIT #2, must be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and Connector C21S and CIRCUIT #2 to SP2 [or SP4] and Connector C22S).

2. 2070-7A. Each circuit must convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to / from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors must be DB-9S type.

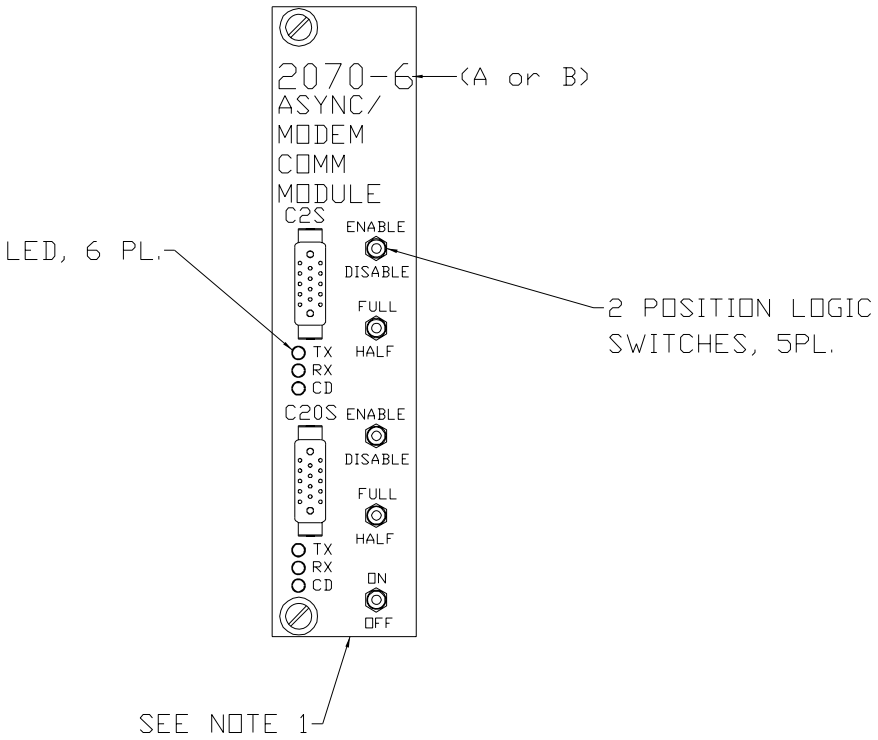
3. 2070-7B. Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground must be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors must be DB-15S type.

4. Indicators. Each circuit signal TX and RX line must have an LED Indicator mounted on the front plate and labeled to function.

D. Details.

Table of Contents

Type 2070-6	-	Async/Modem Serial Comm Module	Figure17
Type 2070-7	-	Serial Comm Module	Figure18



C2 & C20 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	DATA IN
C	AUDIO OUT	L	DATA OUT
D	ISO +5 VDC	M	CTS
E	AUDIO OUT	N	ISO DC GND
F	NA	P	NA
H	CD	R	NA

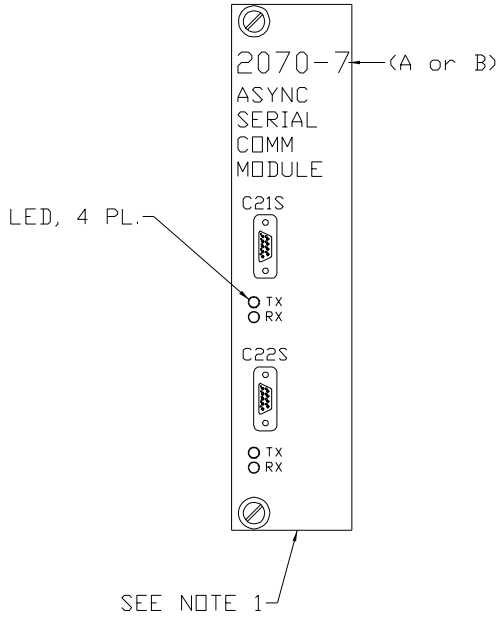
NOTES (THIS DETAIL)

1. 2X Faceplate
(See 2070 System
PCB Module, Detail 9-7-6).

2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.

TITLE: MODEL 2070-6A, 6B ASYNC/MODEM SERIAL COMM MODULE	
Rev Date 2-11-04	10-5-1
FEBRUARY 20, 2004	

Figure 17
Async/Modem Serial Comm Module



2070-7A (DB-9S)	
C21 & C22 CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	ISO DC GND
6	NA
7	RTS
8	CTS
9	NA

2070-7B (DB-15S)			
C21 & C22 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA +	9	TX DATA -
2	ISO DC GND	10	ISO DC GND
3	TX CLOCK +	11	TX CLOCK -
4	ISO DC GND	12	ISO DC GND
5	RX DATA +	13	RX DATA -
6	ISO DC GND	14	ISO DC GND
7	RX CLOCK +	15	RX CLOCK -
8	NA		

NOTES (THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail 9-7-6).

2. Connectors 21 & 22 are DB 9S for Module 7A & DB 15S for Module 7B.

TITLE: MODEL 2070-7A, 7B ASYNC / SYNC SERIAL COMM MODULE	
Rev Date 2-11-04	10-5-2
FEBRUARY 20, 2004	

Figure 18
Serial Comm Module

2.09 NEMA MODULE

A. Type 2070N Controller Unit.

General. This section covers two versions of Type 2070 / NEMA Standard Controller Units. The versions associate with NEMA TS1 and NEMA TS2 Type 1 Standards as described in 3. General Requirements B.

1. Serial Port 5 Frame Address. The Serial Port 5 Frame Address for 2070-2N and 2070-8 must be “20”.

B. 2070-2N Field I/O Module.

1. Interfaces. The 2070-2N Field I/O Module provides a TS2-1 compatible SDLC interface via 2070 Serial Port 3, AC Power to the 2070 Unit and Fault Monitor Logic Output via 2070 Serial Port 5 and Output Frame Byte 9 Bit 6 to the NEMA TS2 Cabinet Monitor Unit (CMU).

2. Type 2070-2N Module Requirements. The Module must meet the 2070–2A Module Requirements with the following exceptions:

   No C1, C11 and C12 Connectors on the front panel of the module
   No 64 inputs / 64 outputs requirements
   Serial Port 5 routed to the FCU MPU Device only
   Serial Port 3 must not have a disabling switch

3. Physical. The module must be a 4X type board / front panel with three connectors. The connectors are 10 Pin Connector A, a NEMA 5-15 Receptacle and a 15 Pin DB 15S C14 Connector.

4. Power. Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle. Connector A must intermate with a NEMA TS2 Type 1 (MS3106O-18-1S) cable.

5. Serial Port 3 Isolation. The module must isolate 2070 Serial Port 3 from the A3 Connector and reconvert the lines to external EIA 485 drivers/receivers that must be terminated at C14 Connector. The Port must be clocked at 153.6 kilobits per second.

6. FCU Output. An FCU output must drive an open collector transistor whose output must be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor must be capable of sinking 200 milliamperes at 30 VDC.

7. Connector Pin Assignments. Connectors A and C14 pin out and functions are as follows:

Connector A

Pin	Function	Pin	Function	Pin	Function
A	AC Neutral	E	NA	I	NA
B	NA	F	Fault Monitor J	NA	
C	AC Line	G	DC#2 Ground		
D	NA	H	Equip Ground		

Connector C14S

Pin	Function	Pin	Function	Pin	Function
1	TX Data+	6	DC Ground	11	TX Clock -
2	DC Ground	7	RX Clock +	12	Equip Ground
3	TX Clock+	8	DC Ground	13	RX Data -
4	DC Ground	9	TX Data -	14	NA
5	RX Data+	10	NA	15	RX Clock –

8. TS2 BIU Control. Serial Port 3 must control the TS2 BIU Units using SDLC Protocol that meets the NEMA TS2 Type 1 Frame Command / Response Standards.

C. 2070-4N (A or B) POWER SUPPLY MODULE.

1. Requirements. The 2070-4N Power Supply Module supports the NEMA TS1 and TS2 Standards. The module is identical to the 2070-4N (A and B) Power Supply Requirements except for the following:

   a. The power cord must have a 15 in. +/- 1 in. length as measured from the panel to the plug tips.

   b. The AC Power Fail voltage must be 85VAC +/-2VAC.

   c. The AC Power Restore voltage must be 90VAC +/-2VAC.

   d. The 2070-4N (A or B) power supply must have proper marking Example “2070 4N (A or B)”. A permanent sticker is an acceptable marking method.

D. Type 2070- 8 Field I/O Module.

1. Type 2070-8 Field I/O Module. The Module consists of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors. The Module CHASSIS must be made of 0.06-inch minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, to be countersunk and be Phillips flat head stainless steel. The matching nuts must be permanently captive on the mating surfaces.

2. Module Front Panel. The MODULE FRONT PANEL must be furnished with the following:

   a. ON/OFF POWER Switch mounted vertically with ON in the UP position.

   b. 2. LED DC Power Indicator. The indicator must indicate that the required
      + 5 VDC is within 5% and the +24 VDC is within 8%.

   c. Incoming VAC fuse protection.

   d. Two DB-25S COMM connectors labeled "EX1" & "EX2."

   e. Four NEMA Connectors A, B, C, & D.

3. Label. A permanent LABEL must be affixed to the Front Panel. The label must display the unit's serial number. The number must be permanent and easy to read.

4. Module Power Supply. A MODULE POWER SUPPLY must be provided and located on the right side of the module as viewed from the front. The supply must provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply must meet the following requirements:

   a. Input Protection (See 10.E.3.).

   b. Power Supply Requirements (See 10.E.6.).

   c. DC Voltage Tolerances. DC Voltage tolerances must be +/-3%.

5. Incoming AC Power. The supplied INCOMING AC POWER must be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC must be at Connector A, Pin "B" and Connector D Pin "NN." AC Power for the 2070 receptacle must be tapped off from the secondary side of the ON Switch / Fuse configuration.

6. Module PC Boards. A MODULE PC Boards must be mounted vertically.

7. Power Down, NRESET, and LINESYNC. Power Down, NRESET, and LINESYNC must be routed to the module via C12 Connector. The state of the module output ports at the time of Power Down transition to LOW State and until NRESET goes HIGH must be an open circuit.

8. Compliance with Type 2070-2 Field I/O Requirements. The Module must meet all requirements under 10.C. with the following exceptions:

    a. Parallel Ports. Parallel Ports, consisting of 118 Bits of Input and 102 bits of Output, must be provided. Specification for inputs applies except the voltage is +24 in lieu of +12 and Ground False, "0," exceeds 16.0 VDC. LINESYNC signal is incoming in differential logic.

    b. Serial Communication Circuitry. The module must interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. All signal lines must be isolated. HAR 1 Harness must be 17 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to the Controller interface, the EIA-485 Signal lines must be routed to EX1 Connector. All necessary driver/receiver and isolation circuitry must be provided.

9. EIA-232 Serial Port. An EIA-232 Serial Port must be provided with rate selection by jumper of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 kilobits per second asynchronous and be connected at EX1 Connector.

10. HAR 2 Harness. A 22-line minimum HAR 2 Harness must be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the Type 2070 UNIT. This provides two Modems or EIA-232 Interfaces with the 2070 UNIT and the outside world.

11. Fault and Voltage Monitor. FAULT and VOLTAGE MONITOR circuitry – NEMA TS1 Controller FAULT and VOLTAGE MONITOR functions (outputs to cabinet monitor) must be provided.

    a. Two 3-input OR gates must be provided. The gate 1 output must be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output must be connected to Connector A, Pin C. Any FALSE state input must cause a gate output FALSE (+24VDC) state.

    b. The FCU Port 10, Bit 7 output must normally change its state every 100 milliseconds. A MODULE Watchdog (WDT) circuit must monitor the output. No state change for 2 +/-0.1 seconds must cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the WDT output must return to TRUE (0 VDC) state.

    c. The module must have a +5 VDC monitoring circuit that monitors the module’s +5 VDC (+/-0.25). If the voltage exceeds the limits, the circuit output must generate a FALSE output (input to gates 1 and 2). Normal operation must return the output state to TRUE state.

    d. The FCU microprocessor output must be assigned to FAULT Monitor (input to gate 1) and another output must be assigned to VOLTAGE Monitor (input to gate 2).

e. CPU Port 5 SET OUTPUT COMMAND Message OUTPUTs O78 and O79 must be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state “1” must be FCU output FALSE.

f. CPU / FCU operation at POWER UP must be as follows:

(1) FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.

(2) CPU REQUEST MODULE STATUS COMMAND Message with “E” bit set is sent to FCU to clear Comm Loss Flag and responds to CPU with “E” bit reset.

(3) Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to “0” will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.

(4) If the above message sequence is not followed, Comm Loss Flag must be set (or remain) and VM & FM must retain the FALSE output state.

(5) Performs items 2 & 3 above User Software.

g. A CPU / FCU Communications Loss during normal operation must cause all outputs to go blank (FALSE state) and must set the Comm Loss Flag. FM and VM outputs must be in FALSE state.

E. Details.

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MODEL 2070N1	-	Side View	Figure20
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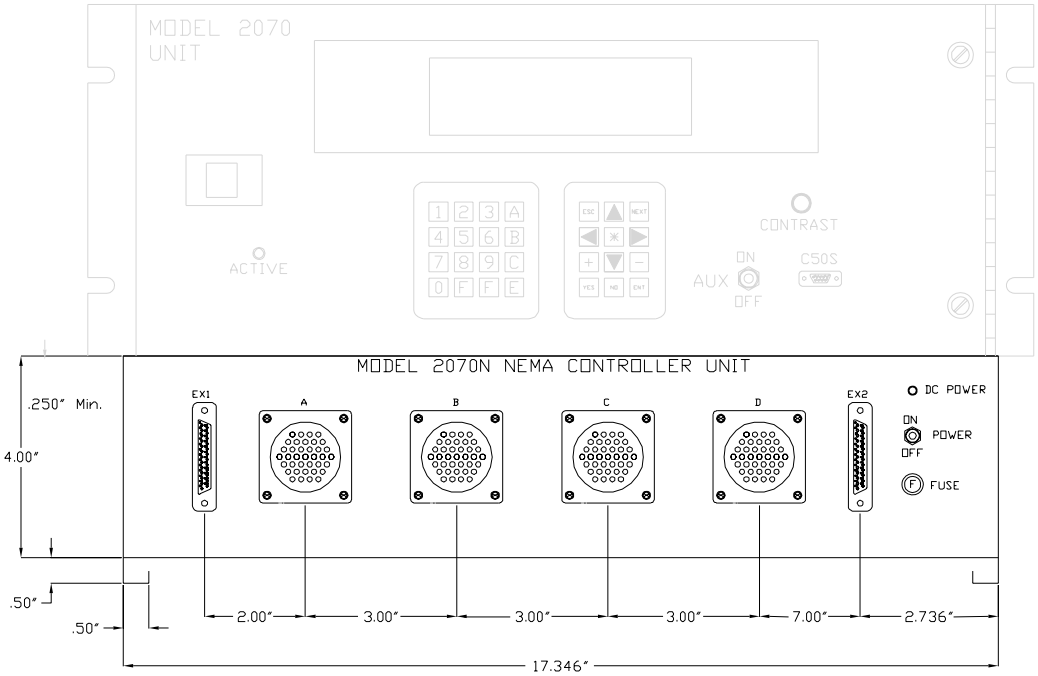
MODEL 2070N1	-	2070-8 Field I/O Module, Connectors C & D	Figure23
MODEL 2070N1	-	2070-8 Field I/O Module, EX1 & EX2 Connectors	Figure24



NOTES (THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for refernce.

2. The bottom supports shall be double flanged.

3. A = Connector A (MS-3112-22-55P Type)
   B = Connector B (MS-3112-22-55S Type)
   C = Connector C (MS-3112-24-61S Type)
   D = Connector D (MS-3112-24-61P Type)
   EX1 = Connector EX1 (DB-25S Type)
   EX2 = Connector EX2 (DB-25S Type)

4. 2.286 mm wide spacers shall be provided between the inside wall of the 2070-8 Module and the 2070 unit (each side).

TITLE: 2070 (V or L) N1 CONTROLLER UNIT FRONT VIEW	
Rev Date 2-11-04	11-5-1
FEBRUARY 20, 2004	

Figure 19
Front View

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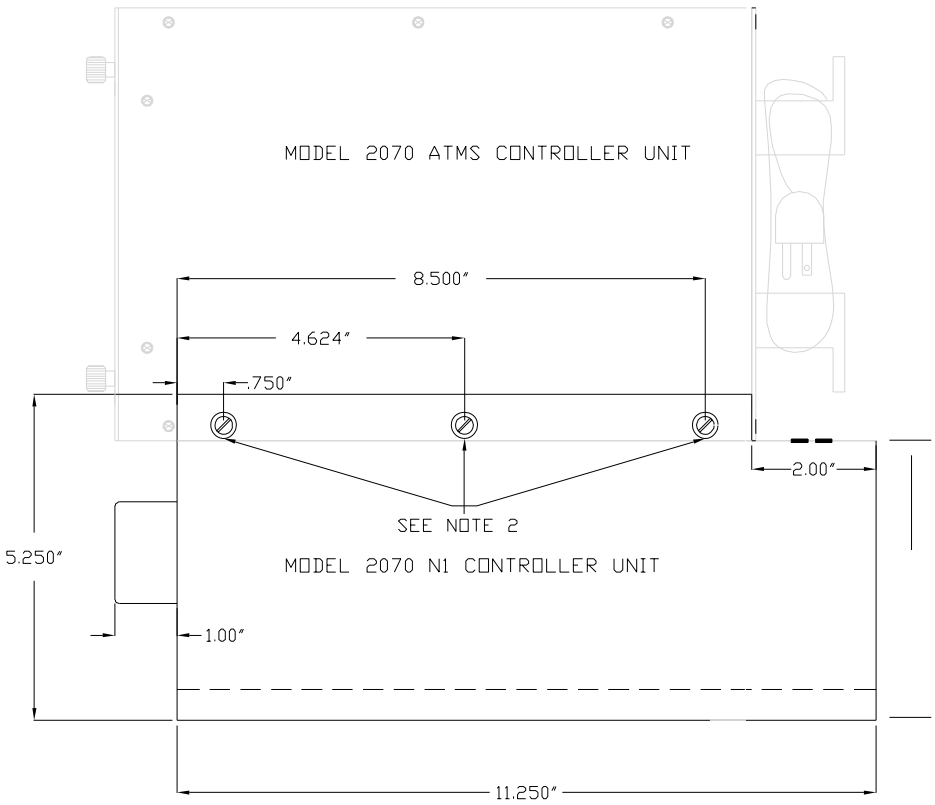
01/14/2008



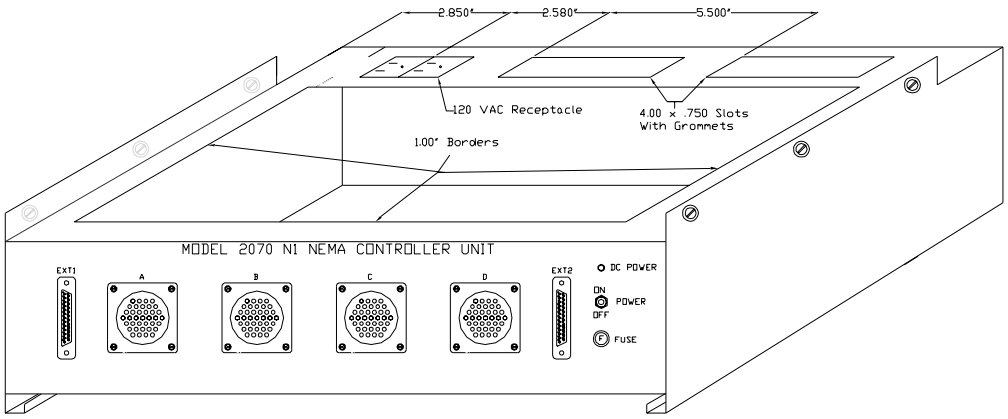
NOTES (THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for reference.
2. TDS #3 Thumbscrew Devices. Module shall provide mating nuts permanently mounted on the module

TITLE: 2070 N1 CONTROLLER UNIT SIDE VIEW	
Rev Date 2-11-04	11-5-2
FEBRUARY 20, 2004	

Figure 20
Side View

16731-103
01/14/2008



NOTES (THIS DETAIL)

1. The module housing bottom shall be slot vented. The top shall be open.

TITLE: 2070 N1 CONTROLLER UNIT ISO VIEW	
Rev Date 2-11-04	11-5-3
FEBRUARY 20, 2004	

Figure 21
Isometric View

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A & B.
Commends shall be available for option 3C (C60).

INQUIRY COMMAND-RESPONSE CODES

COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

TITLE: 2070-8 FIELD I/O MODULE CONNECTORS A & B	
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Figure 22
2070-8 Field I/O Module, Connectors A & B

	CONNECTOR C			CONNECTOR D		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Coded Status Bit A (Ring 2)	Out	12-4	Detector 9	In	10-1
B	Coded Status Bit B (Ring 2)	Out	12-5	Detector 10	In	10-2
C	Phase 8 Don't Walk	Out	4-8	Detector 11	In	10-3
D	Phase 8 Red	Out	1-8	Detector 12	In	10-4
E	Phase 7 Yellow	Out	2-7	Detector 13	In	10-5
F	Phase 7 Red	Out	1-7	Detector 14	In	10-6
G	Phase 6 Red	Out	1-6	Detector 15	In	10-7
H	Phase 5 Red	Out	1-5	Detector 16	In	10-8
J	Phase 5 Yellow	Out	2-5	Detector 17	In	11-1
K	Phase 5 Ped Clear	Out	5-5	Detector 18	In	11-2
L	Phase 5 Don't Walk	Out	4-5	Detector 19	In	11-3
M	Phase 5 Next	Out	8-5	Detector 20	In	11-4
N	Phase 5 On	Out	9-5	Detector 21	In	11-5
P	Phase 5 Vehicle Detector	In	1-5	Detector 22	In	11-6
R	Phase 5 Pedestrian Detector	In	2-5	Detector 23	In	11-7
S	Phase 6 Vehicle Detector	In	1-6	Detector 24	In	11-8
T	Phase 6 Pedestrian Detector	In	2-6	Clock Update	In	12-1
U	Phase 7 Pedestrian Detector	In	2-7	Hardware Control	In	12-2
V	Phase 7 Vehicle Detector	In	1-7	Cycle Advance	In	12-3
W	Phase 8 Pedestrian Detector	In	2-8	Max 3 Selection	In	12-4
X	Phase 8 Hold	In	3-8	Max 4 Selection	In	12-5
Y	Force Off (Ring 2)	In	7-1	Free	In	12-6
Z	Stop Timing (Ring 2)	In	7-2	Not Assigned	In	12-7
a	Inhibit Max Timing (Ring 2)	In	7-3	Not Assigned	In	12-8
b	Test Input C	In	9-3	Alarm 1	In	13-1
c	Coded Status Bit C (Ring 2)	Out	12-6	Alarm 2	In	13-2
d	Phase 8 Walk	Out	6-8	Alarm 3	In	13-3
e	Phase 8 Yellow	Out	2-8	Alarm 4	In	13-4
f	Phase 7 Green	Out	3-7	Alarm 5	In	13-5
g	Phase 6 Green	Out	3-6	Flash In	In	13-6
h	Phase 6 Yellow	Out	2-6	Conflict Monitor Status	In	13-7
i	Phase 5 Green	Out	3-5	Door Ajar	In	13-8
j	Phase 5 Walk	Out	6-5	Special Function 1	In	14-1
k	Phase 5 Check	Out	7-5	Special Function 2	In	14-2
m	Phase 5 Hold	In	3-5	Special Function 3	In	14-3
n	Phase 5 Omit	In	5-5	Special Function 4	In	14-4
p	Phase 6 Hold	In	3-6	Special Function 5	In	14-5
q	Phase 6 Omit	In	5-6	Special Function 6	In	14-6
r	Phase 7 Omit	In	5-7	Special Function 7	In	14-7
s	Phase 8 Omit	In	5-8	Special Function 8	In	14-8
t	Phase 8 Vehicle Detector	In	1-8	Preempt 1 In	In	15-1
u	Red Rest Mode (Ring 2)	In	7-4	Preempt 2 In	In	15-2
v	Omit All Red (Ring 2)	In	7-7	Preempt 3 In	In	15-3
w	Phase 8 Ped Clear	Out	5-8	Preempt 4 In	In	15-4
x	Phase 8 Green	Out	3-8	Preempt 5 In	In	15-5
y	Phase 7 Don't Walk	Out	4-7	Preempt 6 In	In	15-6
z	Phase 6 Don't Walk	Out	4-6	Alarm 1 Out	Out	12-7
AA	Phase 6 Ped Clear	Out	5-6	Alarm 2 Out	Out	12-8
BB	Phase 6 Check	Out	7-6	Special Function 1 Out	Out	13-1
CC	Phase 6 On	Out	9-6	Special Function 2 Out	Out	13-2
DD	Phase 6 Next	Out	8-6	Special Function 3 Out	Out	13-3
EE	Phase 7 Hold	In	3-7	Special Function 4 Out	Out	13-4
FF	Phase 8 Check	Out	7-8	Special Function 5 Out	Out	13-5
GG	Phase 8 On	Out	9-8	Special Function 6 Out	Out	13-6
HH	Phase 8 Next	Out	8-8	Special Function 7 Out	Out	13-7
JJ	Phase 7 Walk	Out	6-7	Special Function 8 Out	Out	13-8
KK	Phase 7 Ped Clear	Out	5-7	Not Assigned	---	---
LL	Phase 6 Walk	Out	6-6	Detector Reset	Out	11-8
MM	Phase 7 Check	Out	7-7	Not Assigned	---	---
NN	Phase 7 On	Out	9-7	+24 VDC	---	---
PP	Phase 7 Next	Out	8-7	2070N DC Gnd	---	---

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Figure 23
2070-8 Field I/O Module, Connectors C & D

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EX1 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD FCU
3	RXD FCU
4	RTS FCU
5	CTS FCU
6	NA
7	2070-8 DC GND
8	DCD FCU
9	2070-8 DC GND
10	485 TX Data+
11	485 TX Data-
12	485 TX Clock+
13	485 TX Clock-
14	2070-8 DC GND
15	485 RX Data+
16	485 RX Data-
17	2070-8 DC GND
18	485 RX Clock+
19	485 RX Clock-
20	NA
21	NA
22	NA
23	NA
24	NA
25	NA

EX2 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD 1
3	RXD 1
4	RTS 1
5	CTS 1
6	NA
7	DC GND #1
8	DCD 1
9	AUDIO IN 1
10	AUDIO IN 1
11	AUDIO OUT 1
12	AUDIO OUT 1
13	NA
14	EQ GND
15	TXD 2
16	RXD 2
17	RTS 2
18	CTS 2
19	NA
20	DC GND #1
21	DCD 2
22	AUDIO IN 2
23	AUDIO IN 2
24	AUDIO OUT 2
25	AUDIO OUT 2

TITLE: 2070-8 FIELD I/O MODULE EX1 & EX2 CONNECTORS	
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Figure 24
2070-8 Field I/O Module, EX1 & EX2 Connectors

2.10 GLOSSARY

A. Terms and Abbreviations. Wherever the following terms or abbreviations are used, the intent and meaning is interpreted as follows:

- A Ampere
- AC Alternating Current
- AC+ 120 Volts AC, 60 hertz ungrounded power source
- AC- 120 Volts AC, 60 hertz grounded return to the power source
- DEPARTMENT The DEPARTMENT director, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them.
- ANSI American National Standard Institute
- ASCII American Standard Code for Information Interchange
- Assembly A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules
- ASTM American Society for Testing and Materials
- AWG American Wire Gage
- C Celsius
- C Language The ANSI C Programming Language
- Cabinet An outdoor enclosure generally housing the controller unit and associated equipment
- Certificate of Compliance A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications
- Channel An information path from a discrete input to a discrete output.

- Component Any electrical or electronic device
- Contractor The person or persons, Manufacturer, firm, partnership, corporation, vendor or combination thereof, who have entered into a contract with the DEPARTMENT, as party of the second part or legal representative
- Controller Unit That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly
- CPU Central Processing Unit
- CTS Clear To Send
- DAT Program The DEPARTMENT's Diagnostic and Acceptance Test Program
- dB Decibel
- dBa Decibels above reference noise, adjusted
- DC Direct Current
- DCD Data Carrier Detect (Receive Line Signal Detector)
- DIN Deutsche Industrie Norm
- DRAM Dynamic random access memory. Random access means that the processor can access any part of the memory or data storage space directly rather than having to proceed sequentially from some starting place. DRAM is dynamic in that it needs to have its storage cells refreshed or given a new electronic charge every few milliseconds.
- EG Equipment Ground
- EIA Electronic Industries Association
- EMI Electro Magnetic Interference

- EPROM Ultraviolet Erasable, Programmable, Read Only Memory Device

- EEPROM Electrically Erasable, Programmable, Read Only Memory Device

- Equal Connectors: comply with physical dimensions, contact material, plating and method of connection. Devices: comply to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device

- ETL Electrical Testing Laboratories, Inc.

- Firmware A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM

- FLASH A +5 VDC powered IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features

- FPA Front Panel Assembly

- HEX Hexadecimal

- Hz Hertz

- IC Integrated Circuit

- I.D. Identification

- IEEE Institute of Electrical and Electronics Engineers

- ISO Isolated

- Jumper A means of connecting/disconnecting two or more conductive by soldering/desoldering a conductive wire or by PCB post jumper

- KB Kilobytes

- Keyed Means by which like connectors can be physically altered to prevent improper insertion.

- Laboratory The established laboratory of the DEPARTMENT or other laboratories authorized by the DEPARTMENT to test materials involved in the contract
- LCD Liquid Crystal Display
- LED Light Emitting Diode
- LOGIC Negative Logic Convention (Ground True) State
- LSB Least Significant Byte
- lsb Least Significant Bit
- MB megabyte
- MSB Most Significant Byte
- msb Most Significant Bit
- m Milli
- MCU/MPU/ IMP Micro Controller Unit, Microprocessor Unit, or Integrated Multiprotocol Processor
- MIL Military Specifications
- MODEM Modulation/Demodulation Unit
- Module A functional unit that plugs into an assembly
- Motherboard A printed circuit connector interface board with no active or passive components
- MOS Metal-Oxide Semiconductor
- MOV Metal-Oxide Varistor
- MS Military Standards

- N Newton: SI unit of force
- N.C. Normally closed contact
- N.O. Normally open contact
- NA Presently Not Assigned. Cannot be used by the Manufacturer for other purposes
- NEMA National Electrical Manufacturer's Association
- NETA National Electrical Testing Association, Inc.
- n nano
- NLSB Next Least Significant Byte
- nlsb Next Least Significant Bit
- NMSB Next Most Significant Byte
- nmsb Next Most Significant Bit
- PCB Printed Circuit Board
- PDA Power Distribution Assembly
- PLA/PAL Programmable Array Logic Device
- Power Failure A Power Failure is said to have occurred when the incoming line voltage falls below 92 +/- 2 VAC for 50 milliseconds. See Power Conditions.
- Power Restoration Power is said to be restored when the incoming line voltage equals or exceeds 97 +/- 2 VAC for 50 milliseconds. See Power Conditions.
- Power Conditions 16.7 ms (one 60 Hertz cycle) reaction period is allowed to be included in the 50 milliseconds timing or added to (67 milliseconds duration). The hysteresis between power failure and power restoration voltage settings must be a min. of 5 VAC with a threshold drift of no more than 0.2 VAC.

- ppm Parts per million
- PWM Pulse Width Modulation
- RAM Random Access Memory
- RF Radio Frequency
- RMS Root-Mean-Square
- ROM Read Only Memory Device
- RTS Request to Send
- R/W Controller Unit Read/Write Control Line
- RxD Received Data
- SCI Serial Communications Interface
- SDLC Synchronous Data Link Control
- S Logic State
- s second
- Second Sourced Produced by more than one Manufacturer
- SRAM Static Random Access Memory Device
- SW Switch
- TB Terminal Block
- TOD Time Of Day Clock
- Triac Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit
- TTL Transistor-Transistor Logic

- Thumb Screw Device (TSD) A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No.2 must be flat black.)

  TSD No.1 - 8-32 SOUTHCO #47-62-301-20 or equal.
  TSD No.2 - 8-32 SOUTHCO #47-62-301-60 or equal.
  TSD No.3 - M3 SOUTHCO #47-82-101-10 or equal.

- TxD Transmitted Data

- u Micro

- UL Underwriter's Laboratories, Inc.

- VAC Voltage Alternating Current (root mean square)

- VDC Voltage Direct Current

- VME Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2

- x Number Value

- XX Manufacturer's Option

- WDT Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts